PNP TRANSISTORS

BJT Transistor Modeling

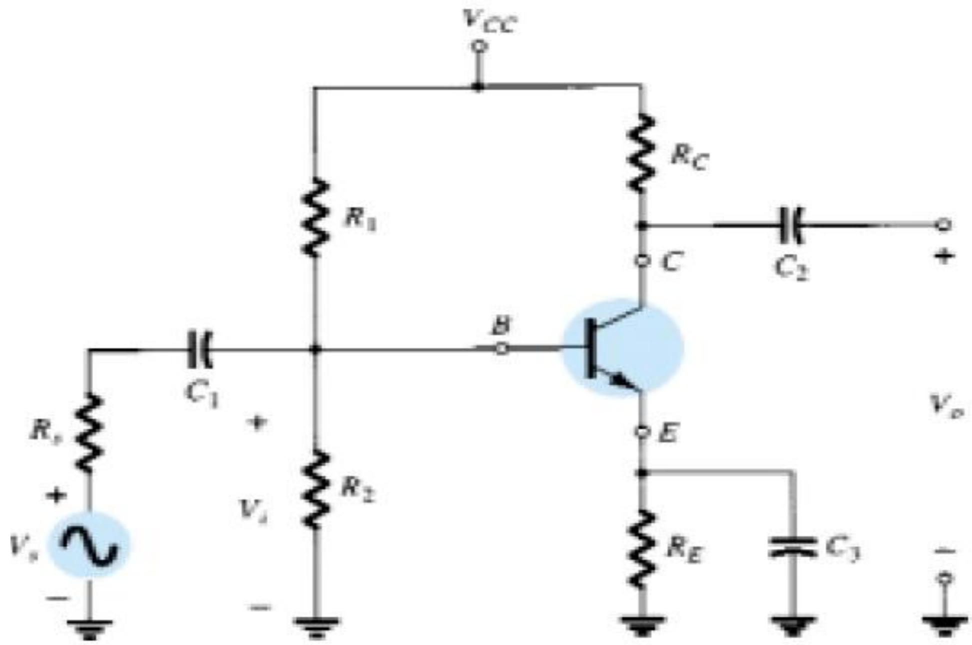

Fig.1:

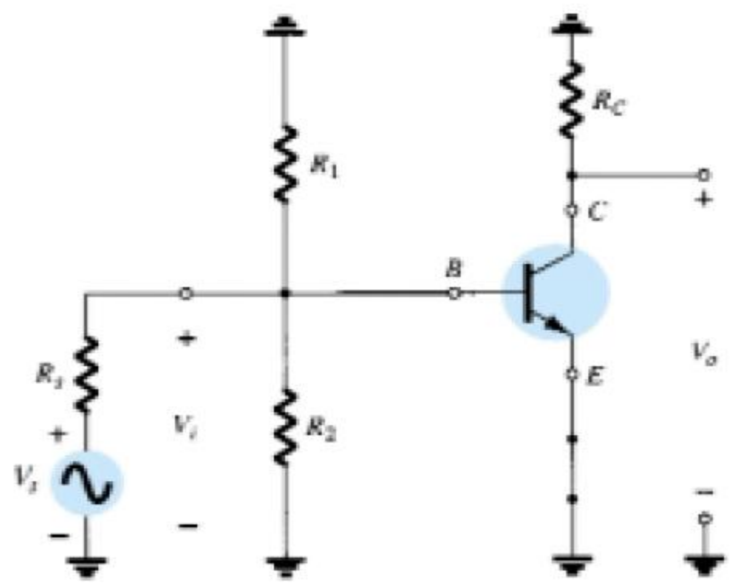

Fig.2: removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

*R*1 and *R*2 will be in parallel and *RC* will appear from collector to emitter as shown in Fig.3. Analysis techniques such as superposition, Thévenin's theorem, and so on, can be appliedto determine the desired quantities.Let us further examine Fig.4 and identify the important quantities to be determined for the system. Since we know that the transistor is an amplifying device, we would expect some indication of how the output voltage $V_o$is related to the input voltage Vi—the *voltage gain*. Note in Fig. 3 for this configuration that $I_i= I_b$and $I_o=I_c$, which define the *current gain* $A_i=I_o/I_i$. The input impedance $Z_i$and output impedance $Z_o$will prove particularly important in the analysis to follow. A great deal more will be offered about these parameters in the sections to follow.

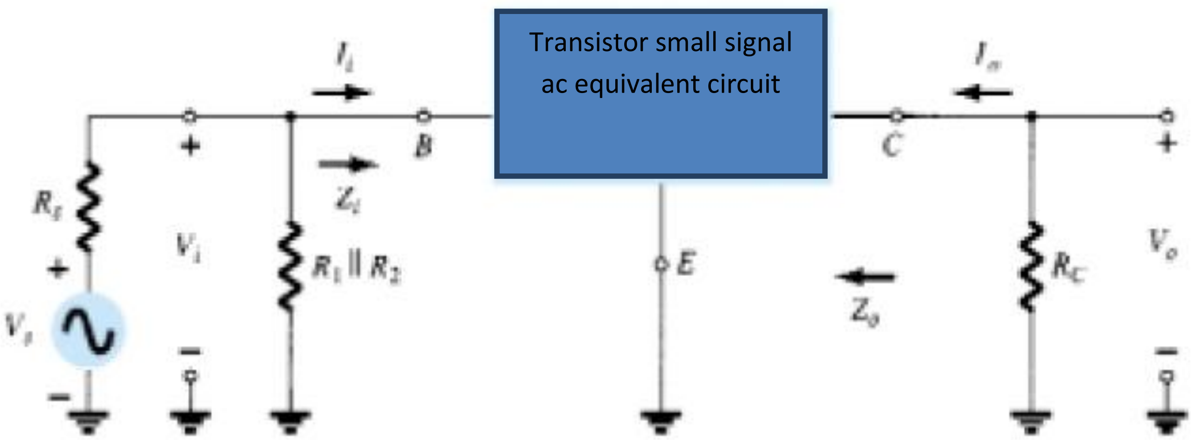

Fig.3: Circuit of Fig.2 redrawn for small-signal ac analysis.

In summary, therefore, the ac equivalent of a network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

THE IMPORTANT PARAMETERS: *Zi, Zo, Av, Ai*

For most electrical and electronic systems, the general flow is usually from the left to the right. For both sets of terminals, the impedance between each pair of terminals under normal operating conditions is quite important.

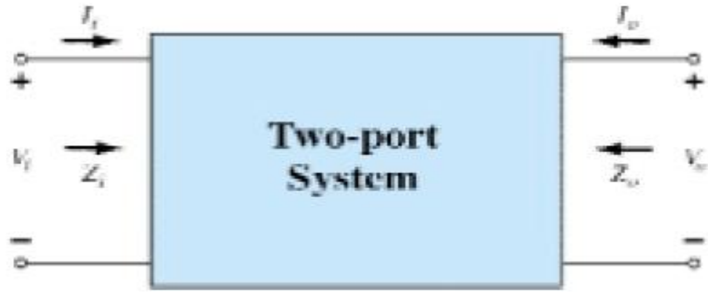

Fig.4: Two-port system.

Input Impedance, *Zi*

For the input side, the input impedance *Zi*is defined by Ohm's law as the following:

$$\boxed{Z_i = \frac{V_i}{I_i}}$$

For small-signal analysis, once the input impedance has been determined the same numerical value can be used for changing levels of applied signal.

The input impedance of a BJT transistor amplifier is purely resistive in nature and, depending on the manner in which the transistor is employed, can vary from a few ohms to megohms.

Both voltages can be the peak-to-peak, peak, or rms values, as long as both levels use the same standard. The input impedance is then determined in the following manner:

$$\boxed{I_i = \frac{V_s - V_i}{R_{\text{sense}}}}$$

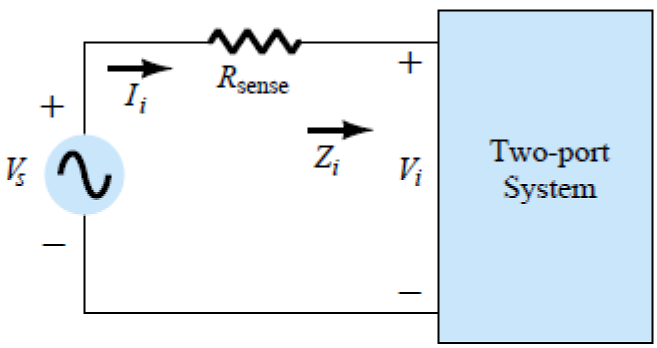

Fig.5: Determining *Zi*.

Output Impedance, *Zo*

The output impedance is determined at the output terminals looking back into the system with the applied signal set to zero.

In Fig.6, for example, the applied signal has been set to zero volts. To determine *Zo*, a signal, *Vs*, is applied to the output terminals and the level of *Vo*is measured with an oscilloscope or sensitive DMM. The output impedance is then determined in the following manner.

$$I_o = \frac{V - V_o}{R_{\text{sense}}}$$

$$Z_o = \frac{V_o}{I_o}$$

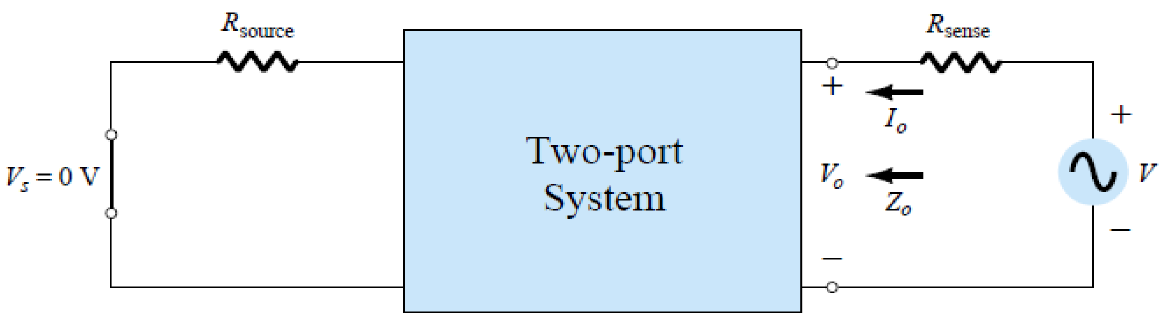

Fig.6: Determining *Zo*.

The output impedance of a BJT transistor amplifier is resistive in nature and, depending on the configuration and the placement of the resistive elements, Zo, can vary from a few ohms to a level that can exceed 2 MΩ.

Voltage Gain, *Av*

$$A_v = \frac{V_o}{V_i}$$

The equation is referred to as the no-load voltage gain. That is,

$$A_{v_{NL}} = \left.\frac{V_o}{V_i}\right|_{R_L = \infty\ \Omega \text{ (open circuit)}}$$

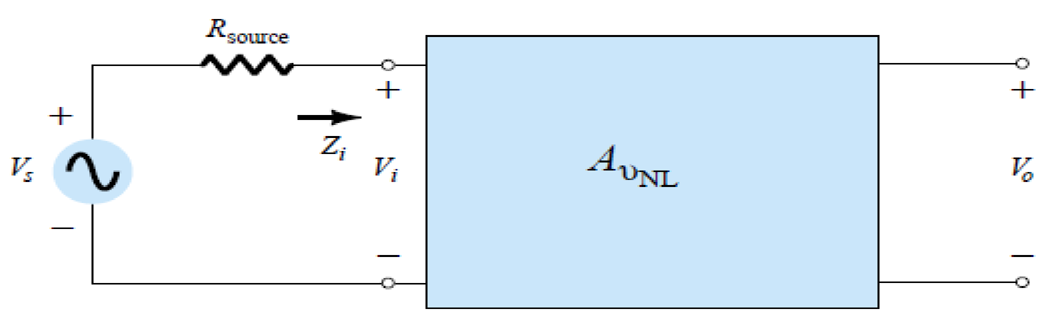

Fig.7:Determining the no-load voltage gain.

For transistor amplifiers, the no-load voltage gain is greater than the loaded voltage gain.

For the system of Fig.7 having a source resistance *Rs*, the level of *Vi* would first have to be determined using the voltage-divider rule before the gain *Vo*/*Vs* could be calculated. That is,

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i}$$

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}}}$$

Example 7.3: For the BJT amplifier of Fig.8, determine:

(a) *Vi*. (b) *Ii*. (c) *Zi*. (d) Av_s.

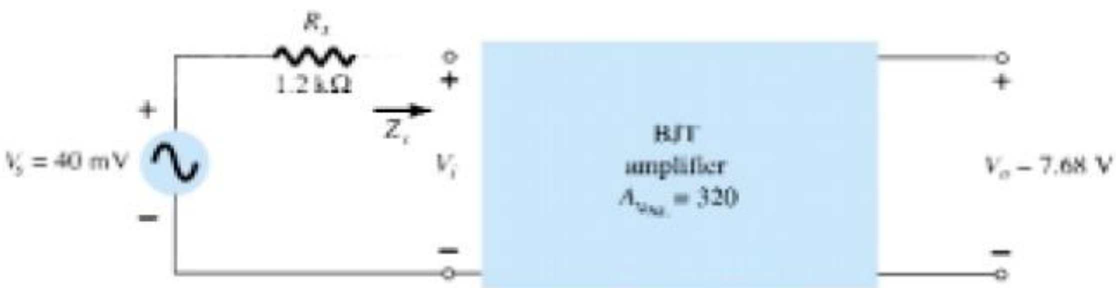

Fig.8

Solution

(a) $A_{v_{NL}} = \frac{V_o}{V_i}$ and $V_i = \frac{V_o}{A_{v_{NL}}} = \frac{7.68\text{ V}}{320} = \mathbf{24\text{ mV}}$

(b) $I_i = \frac{V_s - V_i}{R_s} = \frac{40\text{ mV} - 24\text{ mV}}{1.2\text{ k}\Omega} = \mathbf{13.33\ \mu A}$

(c) $Z_i = \frac{V_i}{I_i} = \frac{24\text{ mV}}{13.33\ \mu\text{A}} = \mathbf{1.8\text{ k}\Omega}$

(d) $A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}}$

$$= \frac{1.8\text{ k}\Omega}{1.8\text{ k}\Omega + 1.2\text{ k}\Omega}(320)$$

$$= \mathbf{192}$$

Current Gain, *Ai*

$$\boxed{A_i = \frac{I_o}{I_i}}$$

For BJT amplifiers, the current gain typically ranges from a level just less than 1 to a level that may exceed 100.

For the loaded situation of Fig.:9

$$I_i = \frac{V_i}{Z_i} \qquad \text{and} \qquad I_o = -\frac{V_o}{R_L}$$

Fig.9: Determining the loaded current gain.

with
$$A_i = \frac{I_o}{I_i} = -\frac{V_o/R_L}{V_i/Z_i} = -\frac{V_o Z_i}{V_i R_L}$$

and
$$\boxed{A_i = -A_v \frac{Z_i}{R_L}}$$

THE r_e TRANSISTOR MODEL

Common Emitter Configuration

For the common-emitter configuration of Fig. 10a, the input terminals are the base and emitter terminals, but the output set is now the collector and emitter terminals. In addition, the emitter terminal is now common between the input and output ports of the amplifier. Substituting the *re* equivalent circuit for the *npn* transistor will result in the configuration of Fig. 10b. Note that the controlled-current source is still connected between the collector and base terminals and the diode between the base andemitter terminals.

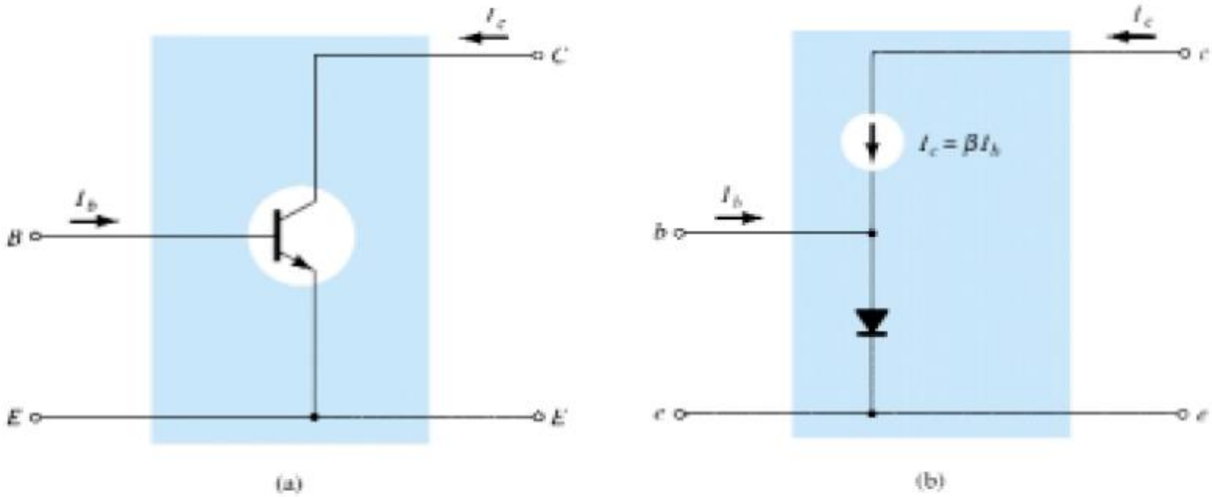

Fig.10: (a) Common-emitter BJT transistor; (b) approximate model

$$\boxed{I_c = \beta I_b}$$

The current through the diode is therefore determined by

$$I_e = I_c + I_b = \beta I_b + I_b$$

and

$$\boxed{I_e = (\beta + 1)I_b}$$

$$\boxed{I_e \cong \beta I_b}$$

The input impedance is determined by the following ratio:

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

The voltage $V_{be}$is across the diode resistance as shown in Fig.11. The level of $r_e$is still determined by the dc current I_E. Using Ohm's law gives

$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$

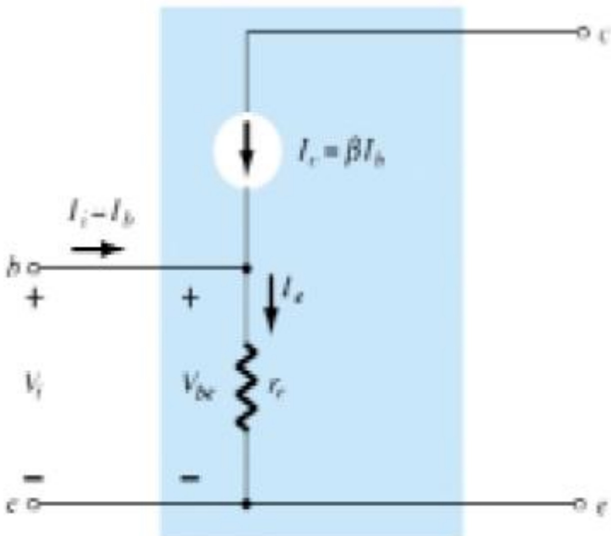

Fig.11: Determining Z_i using the approximate model.

Substituting yields

$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

and

$$\boxed{Z_i \cong \beta r_e} \quad CE$$

For the output impedance,the characteristics of interest are the output set of Fig.12. Note that the slope of the curves increases with increase in collector current. The steeper the slope, the less the level of output impedance (*Zo*). The *re* model of Fig.10 does not include an output impedance, but if available from a graphical analysis or from data sheets, it can be included as shown in Fig.13.

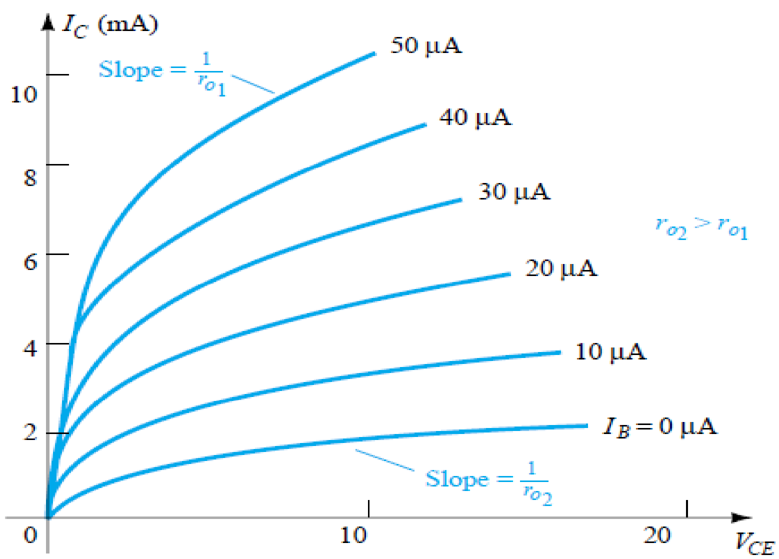

Fig.12: Defining *ro* for the common-emitter configuration.

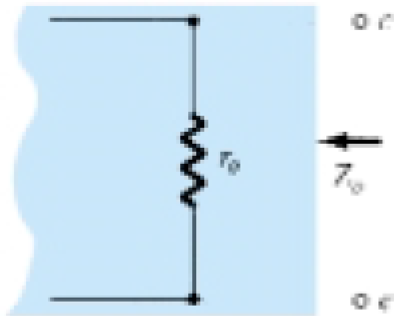

Fig.13: Including $r_o$in the transistor equivalent circuit.

For the model of Fig.13, if the applied signal is set to zero, the current *Ic* is 0 A and the output impedance is

$$\boxed{Z_o = r_o}_{CE}$$

Of course, if the contribution due to r_o is ignored as in the *re* model, the output impedance is defined by $Zo = \infty\Omega$.

The voltage gain for the common-emitter configuration will now be determined for the configuration of Fig.14 using the assumption that $Zo = \infty\ \Omega$. For the defined direction of I_o and polarity of V_o,

$$V_o = -I_oR_L$$

Fig.14: Determining the voltage and current gain for the common-emitter transistor amplifier.

$$V_o = -I_oR_L = -I_cR_L = -\beta I_bR_L$$

and

$$V_i = I_iZ_i = I_b\beta r_e$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_bR_L}{I_b\beta r_e}$$

and

$$\boxed{A_v = -\frac{R_L}{r_e}}_{CE, r_o = \infty\Omega}$$

The resulting minus sign for the voltage gain reveals that the output and input voltages are 180° out of phase.The current gain for the configuration of Fig.14

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

and $$\boxed{A_i = \beta} \quad _{CE, r_o = \infty\ \Omega}$$

Using the facts that the input impedance is r_e, the collector current is I_b, and the output impedance is r_o, the equivalent model of Fig.15 can be an effective tool in the analysis to follow. For typical parameter values, the common-emitter configuration can be considered one that has a moderate level of input impedance, a high voltage and current gain, and output impedance that may have to be included in the network analysis.

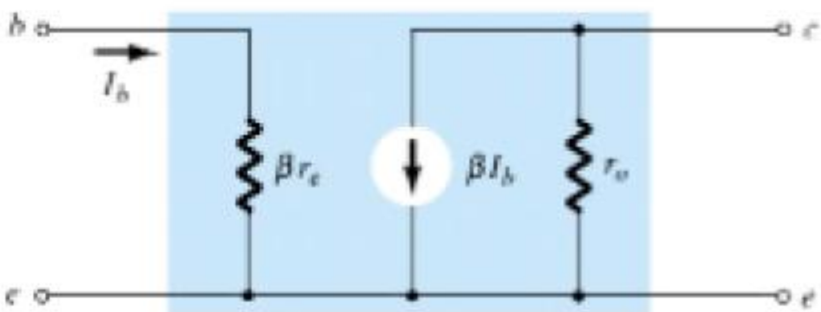

Fig.15: *re* model for the common-emitter transistor configuration.

EXAMPLE. 7.5: Given β = 120 and I_E= 3.2 mA for a common-emitter configuration with *ro* = ∞, assume V_{be} = 26 mV

determine: (a) *Zi*. (b) *Av* if a load of 2 kΩis applied. (c) *Ai* with the 2 kΩ load.

Solution

(a) $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{3.2\text{ mA}} = 8.125\ \Omega$$

and $$Z_i = \beta r_e = (120)(8.125\ \Omega) = \mathbf{975\ \Omega}$$

(b) $$A_v = -\frac{R_L}{r_e} = -\frac{2\text{ k}\Omega}{8.125\ \Omega} = \mathbf{-246.15}$$

(c) $$A_i = \frac{I_o}{I_i} = \beta = \mathbf{120}$$

THE HYBRID EQUIVALENT MODEL

The *re* model for a transistor is sensitive to the dc level of operation of the amplifier. The result is an input resistance that will vary with the dc operating point. For the hybrid equivalent model to be described in this section, the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier. This is due to the fact that specification sheets cannot provide parameters for an equivalent circuit at every possible operating point. The quantities *hie*, *hre*, *hfe*, and *hoe* are called the hybrid parameters

		Min.	Max.	
Input impedance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz) 2N4400	h_{ie}	0.5	7.5	kΩ
Voltage feedback ratio (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz) 2N4400	h_{fe}	20	250	—
Output admittance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{oe}	1.0	30	1μS

Fig. 16: Hybrid parameters for the 2N4400 transistor.

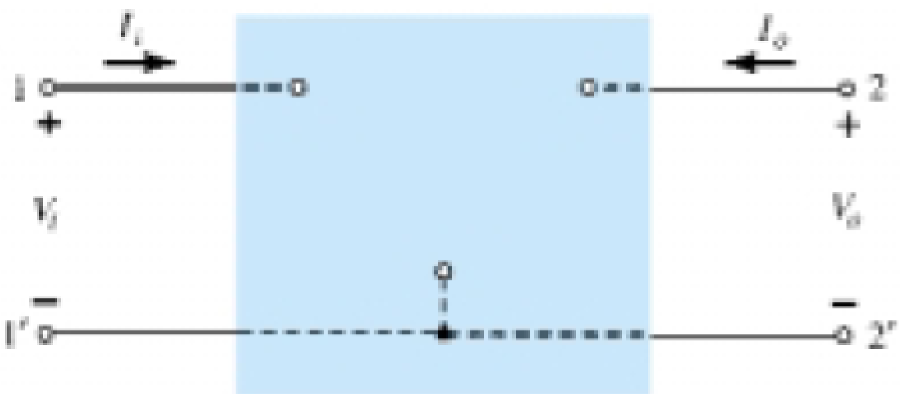

Fig.17: Tow port system

$$\boxed{V_i = h_{11} I_i + h_{12} V_o}$$

$$\boxed{I_o = h_{21} I_i + h_{22} V_o}$$

If we arbitrarily set $V_o = 0$ (short circuit the output terminals) and solve for $h11$, the following will result:

$$\boxed{h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o = 0}} \quad \text{ohms}$$

The ratio indicates that the parameter $h11$ is an impedance parameter with the units of ohms. Since it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted*, it is called the *short-circuit input-impedance parameter*. The subscript 11 of $h11$ defines the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

If Ii is set equal to zero by opening the input leads, the following will result for $h12$:

$$\boxed{h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i = 0}} \qquad \text{unitless}$$

The parameter $h12$, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units since it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter.*

If Vo is equal to zero by again shorting the output terminals, the following will result for $h21$:

$$\boxed{h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}} \qquad \text{unitless}$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for $h12$. The parameter $h21$ is the ratio of the output current to the input current with the output terminals shorted. This parameter, like $h12$, has no units since it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter.*

The last parameter, $h22$, can be found by again opening the input leads to set $I1 = 0$ and solving for $h22$

$$\boxed{h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}} \qquad \text{siemens}$$

Since it is the ratio of the output current to the output voltage, it is the output conductance parameter and is measured in siemens (S). It is called the *open-circuit output admittance parameter.*

let us apply Kirchhoff's voltage law in reverse" to find a circuit in Fig.17 that "fits" the equation

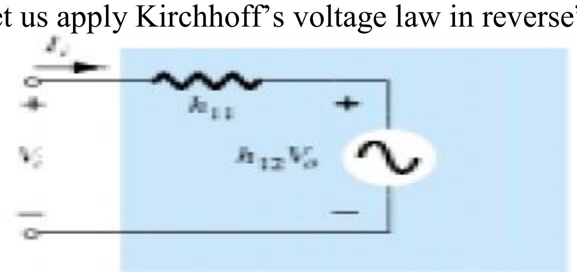

Fig.17: Hybrid input equivalent circuit.

let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 18.

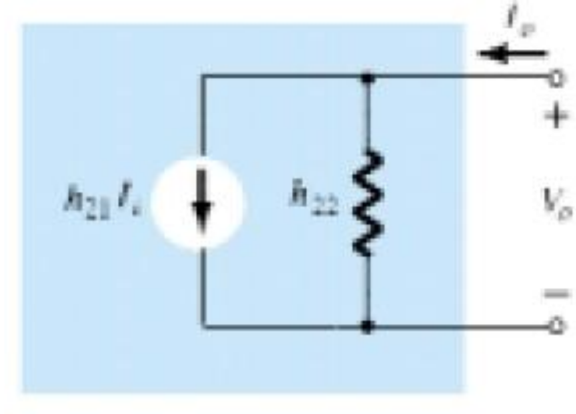

Fig.18: Hybrid output equivalent circuit.

The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig.19 with a new set of subscripts for the *h*-parameters. The notation of Fig.19 is of a more practical nature since it relates the *h*-parameters.

$h11 \rightarrow$ *i*nput resistance $\rightarrow hi$
$h12 \rightarrow$ *r*everse transfer voltage ratio $\rightarrow hr$

$h21 \rightarrow$ *f*orward transfer current ratio $\rightarrow hf$
$h22 \rightarrow$ *o*utput conductance $\rightarrow ho$

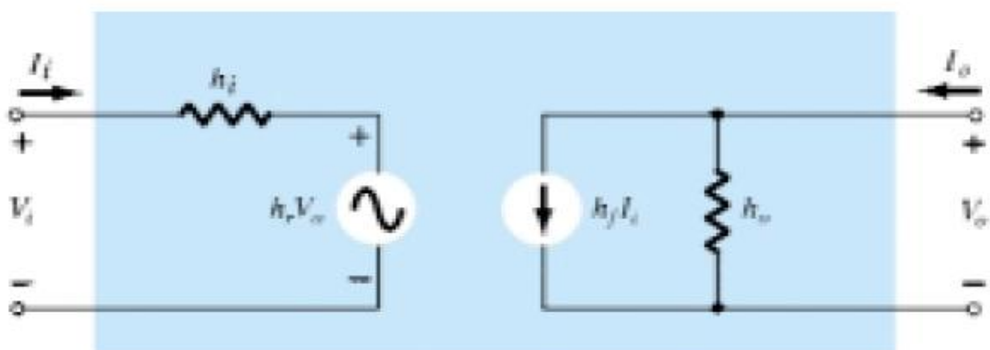

Fig.19: Complete hybrid equivalent circuit.

The fact that both a Thévenin and Norton circuit appear in the circuit of Fig.19 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit

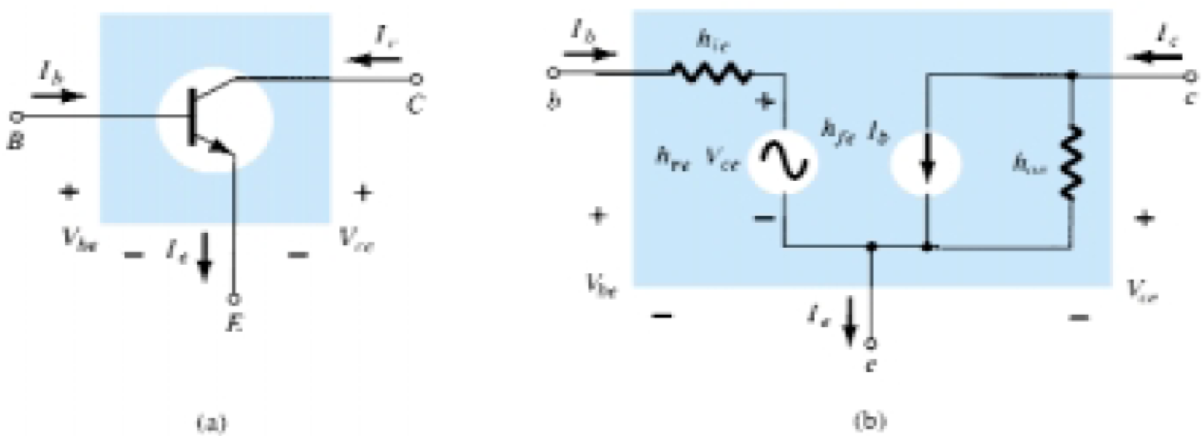

Fig.20: Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.