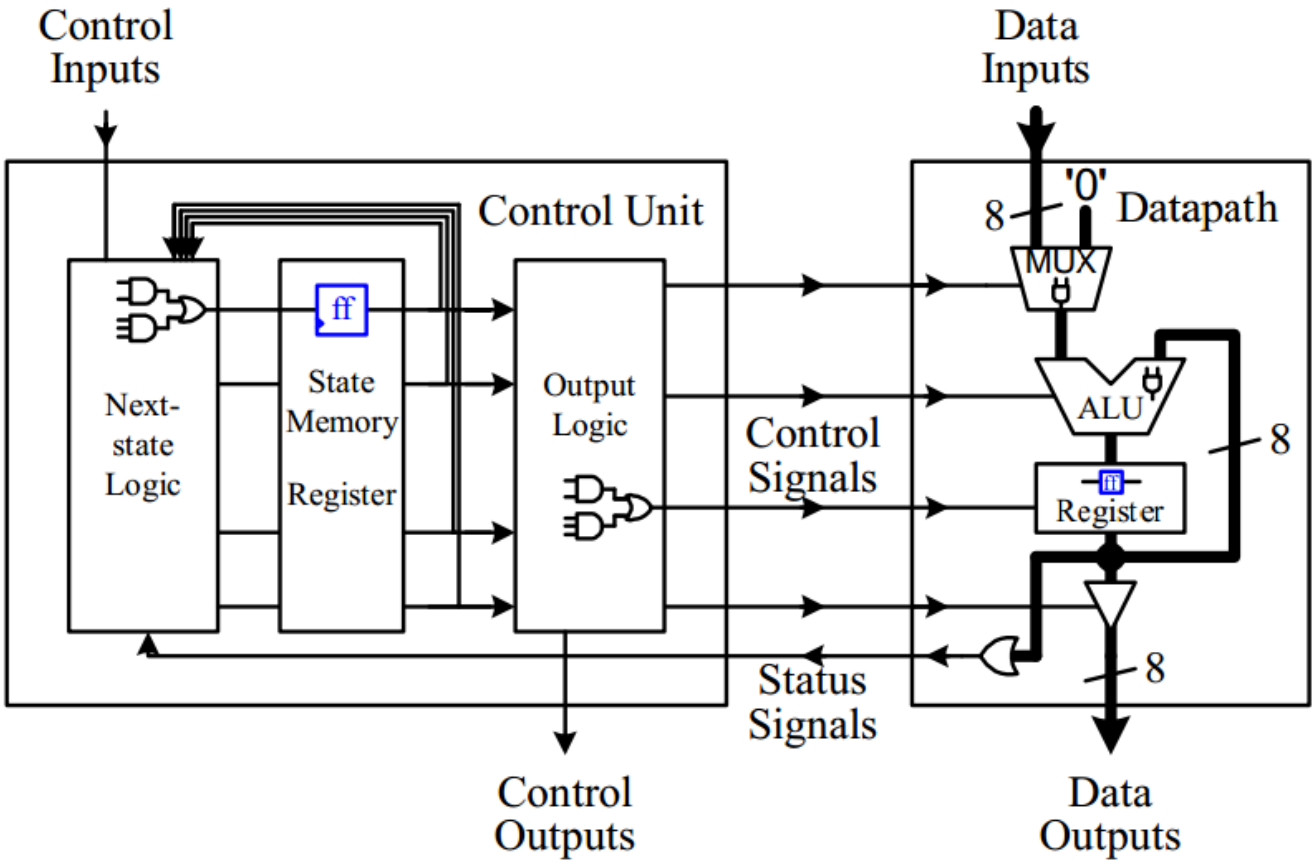
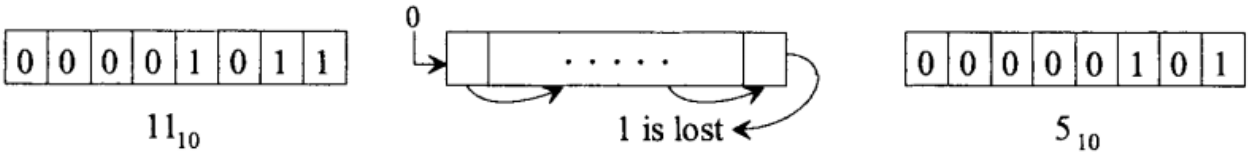
Register

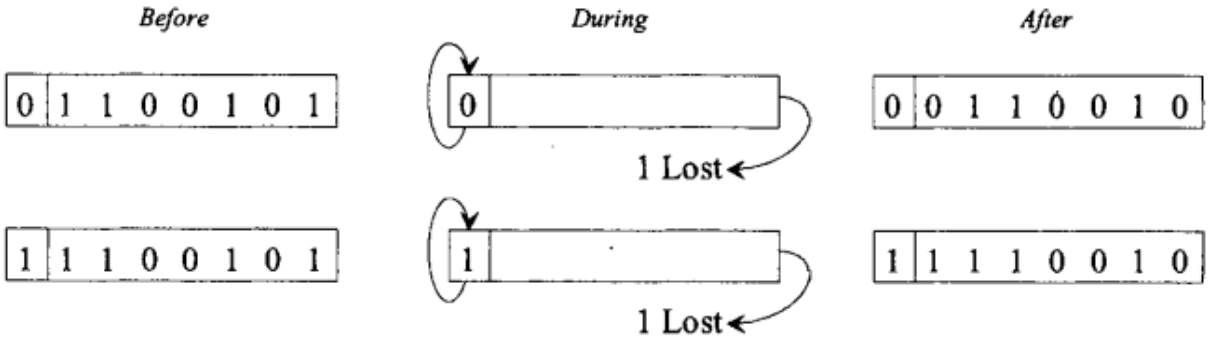

Control Inputs
Data Inputs
Control Unit
Next-state Logic
ff
State Memory Register
Output Logic
Control Signals
Status Signals
'0'
8
MUX
ALU
Register
Datapath
Control Outputs
Data Outputs

Register

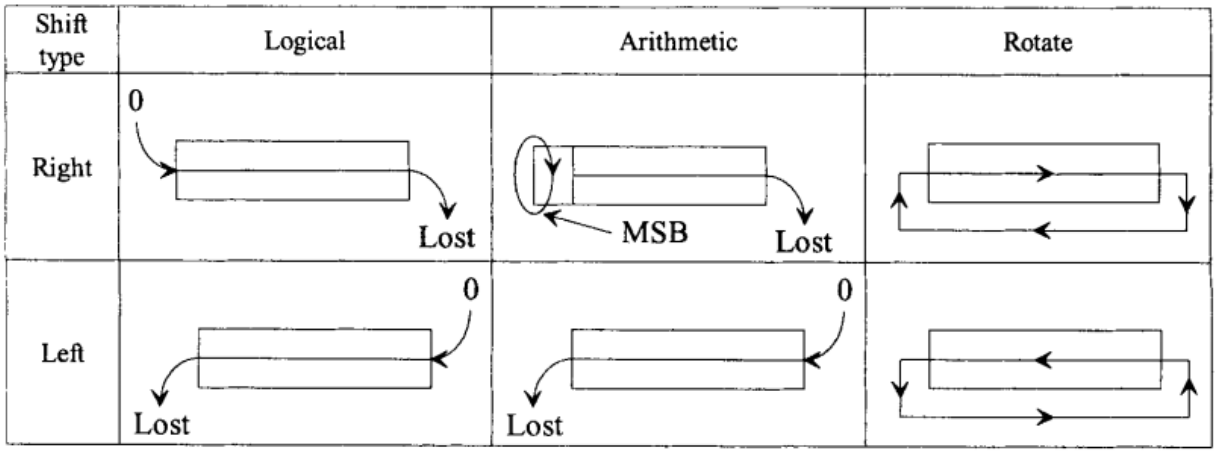
A register contains a number of flip-flops for storing binary information in a computer. The register is an important part of any CPU. A CPU with many registers reduces the number of accesses to the main memory, therefore simplifying the programming task and shortening execution time. A general-purpose register (GPR) is designed in this section. The primary task of the GPR is to store address or data for an indefinite amount of time, then to be able to retrieve the data when needed. A GPR is also capable of manipulating the stored data by shift left or right operations. Figure 5.39 contains a summary of typical shift operations. In logical shift operation, a bit that is shifted out will be lost, and the vacant position will be filled with a 0. For example, if we have the number (1 l),,, after right shift, the following occurs:



It must be emphasized that a logical left or right shift of an unsigned number by n positions implies multiplication or division of the number by 2", respectively, provided that a 1 is not shifted out during the operation. In the case of true arithmetic left or right shift operations, the sign bit of the number to be shifted must be retained. However, in computers, this. is true for right shift and not for left shift operation. For example, if a register is shifted right arithmetically, the most significant bit (MSB) of the register is preserved, thus ensuring that the sign of the number will remain unchanged. This is illustrated next:



There is no difference between arithmetic and logical left shift operations. If



Summary of Typical Shift Operations

Shift registers

Introduction

Shift registers area type of sequential logic circuit, mainly for storage of digital data. They are a group of flip -flops connected in a chain so that the output from one flip -flop becomes the input of the next flip -flop. Most of the registers possess no characteristic internal sequence of states. All flip -flop is driven by a common clock, and all are set or reset simultaneously.

In these few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In -Parallel Out, Parallel In –Serial Out, Parallel In -Parallel Out, and bidirectional shift registers. A special form of counter -the shift register counter, is also introduced.

Storage Capacity:

The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

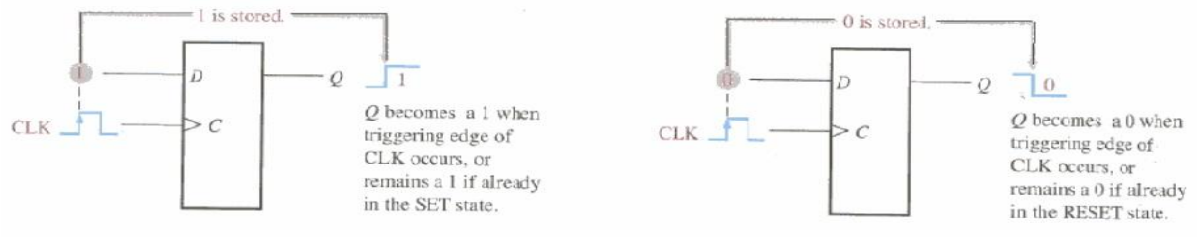


Figure 1: The flip -flop as a storage element.

1. Serial In -Serial Out Shift Registers

The serial in/serial out shift register accepts data serially –that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

1.1 Example: Basic four - bit shift register

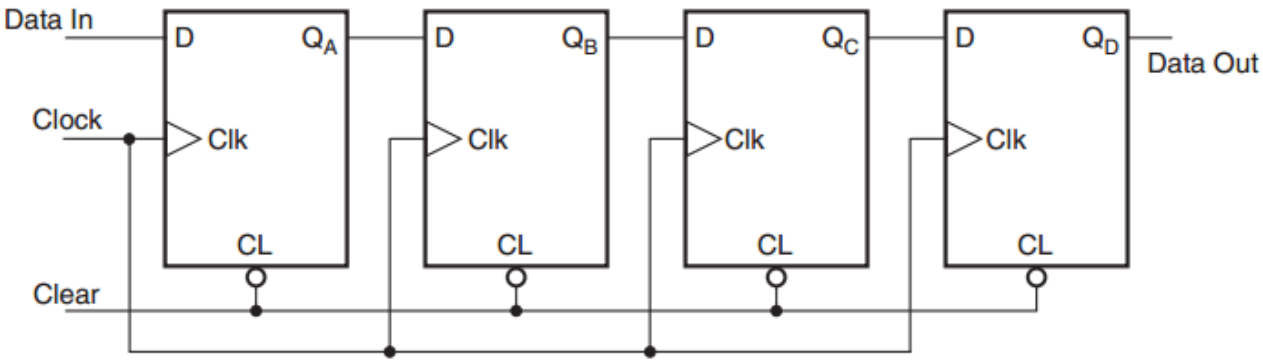
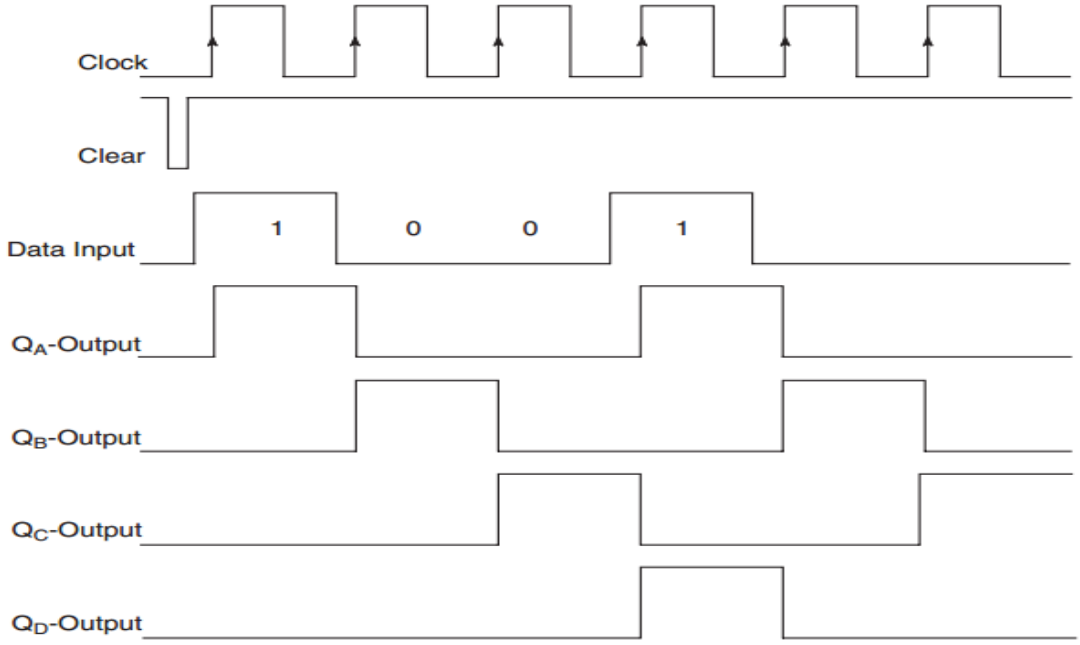


Figure 2.



Timing waveforms for the shift register

The outputs of the other three flip-flops remain in the logic ‘0’ state as their D inputs were in the logic‘0’ state at the time of clock transition. During the second clock transition, the QA output goes from logic ‘1’ to logic ‘0’ and the QB goes from logic ‘0’ to logic ‘1’, again in accordance with the logic status of the D inputs at the time of relevant clock transition.

Thus, we have seen that a logic '1' that was present at the data input prior to the occurrence of the first clock transition has reached the QB output at the end of two clock transitions. This bit will reach the QD output at the end of four clock transitions. In general, in a four-bit shift register of the type A basic four-bit shift register can be constructed using four D flip - flops, as shown in Figure 2.

2. Serial In -Parallel Out Shift Registers

For this kind of register, data bits are entered serially in the same manner as discussed in the last section. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in -parallel out register is shown below.

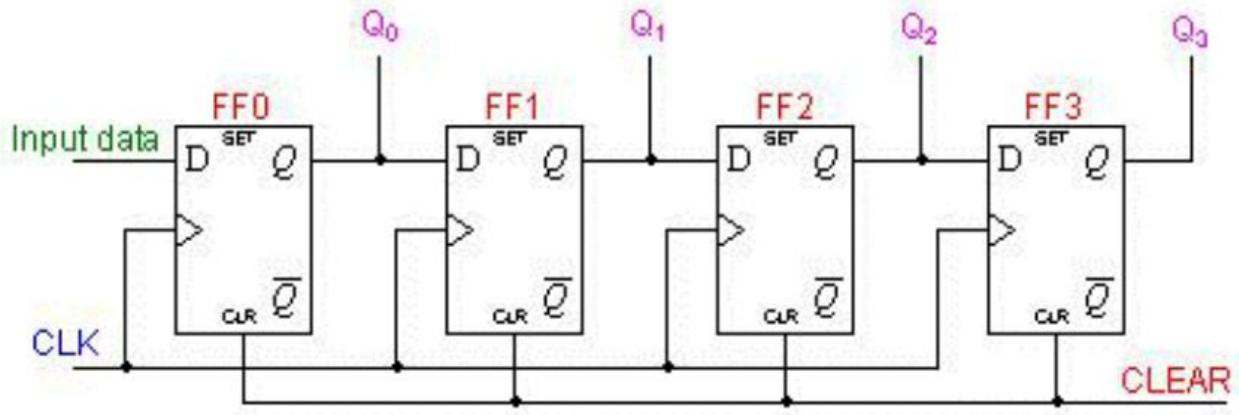


Figure 3.

In the table below, we can see how the four-bit binary number 1001 is shifted to the Q outputs of the register.

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

3. Parallel In -Parallel Out Shift Registers

For parallel in -parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in -parallel out shift register constructed by D flip -flops.

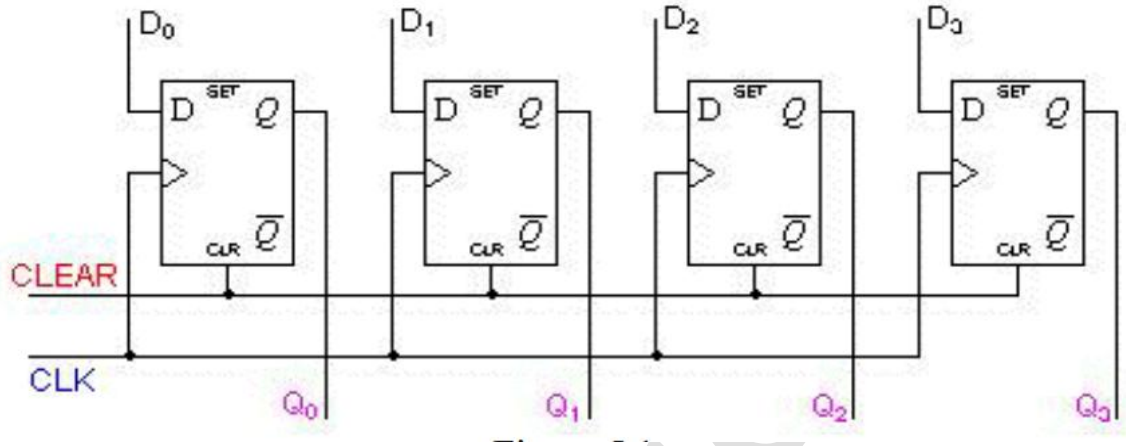


Figure 4.

The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

4. Parallel In -Serial Out Shift Registers

A four-bit parallel in -serial out shift register is shown below. The circuit uses D flip -flops and NAND gates for entering data (ie writing) to the register.

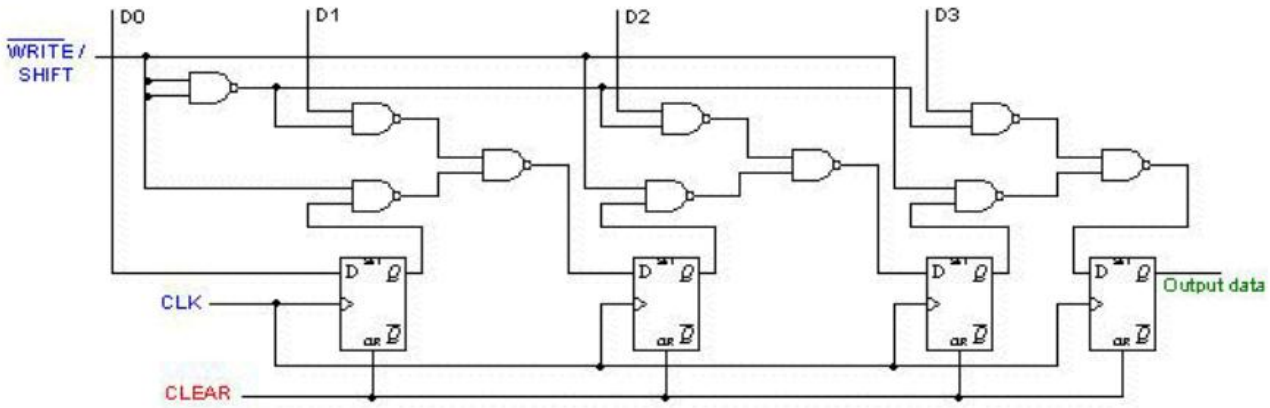


Figure 5.

D0, D1, D2 and D3 are the parallel inputs, where D0 is the most significant bit and D3 is the least significant bit. To write data in, the mode control line is taken to LOW and the data is clocked in. The data can be shifted when the mode control line is HIGH as SHIFT is active high. The register performs right shift operation on the applicat ion of a clock pulse, as shown in the table below.

	Q_0	Q_1	Q_2	Q_3	
Clear	0	0	0	0	
Write	1	0	0	1	
Shift	1	0	0	1	
	1	1	0	0	1
	1	1	1	0	01
	1	1	1	1	001
	1	1	1	1	1001

5. Bidirectional Shift Registers

The registers discussed so far involved only right shift operations. Each right shift operation has the effect of successively dividing the binary number by two. If the operation is reversed (left shift), this has the effect of multiplying the number by two. With suitable gating arrangement a serial shift register can perform both operations. A bidirectional, or reversible, shift register is one in which the data can be shift either left or right. A four-bit bidirectional shift register using D flip-flops is shown below.

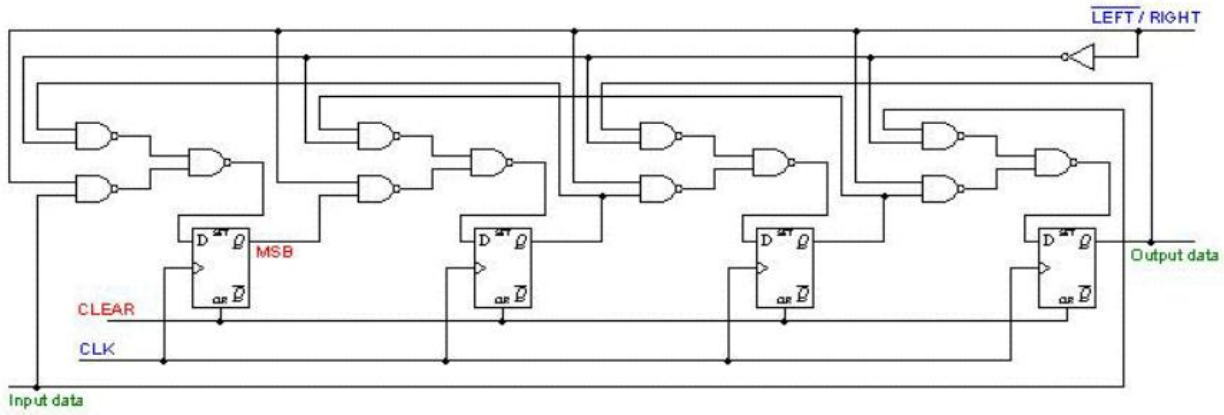


Figure 6.

Here a set of NAND gates are configured as OR gates to select data inputs from the right or left adjacent bistables, as selected by the LEFT/RIGHT control line.

Alternative Circuit: [Floyd]

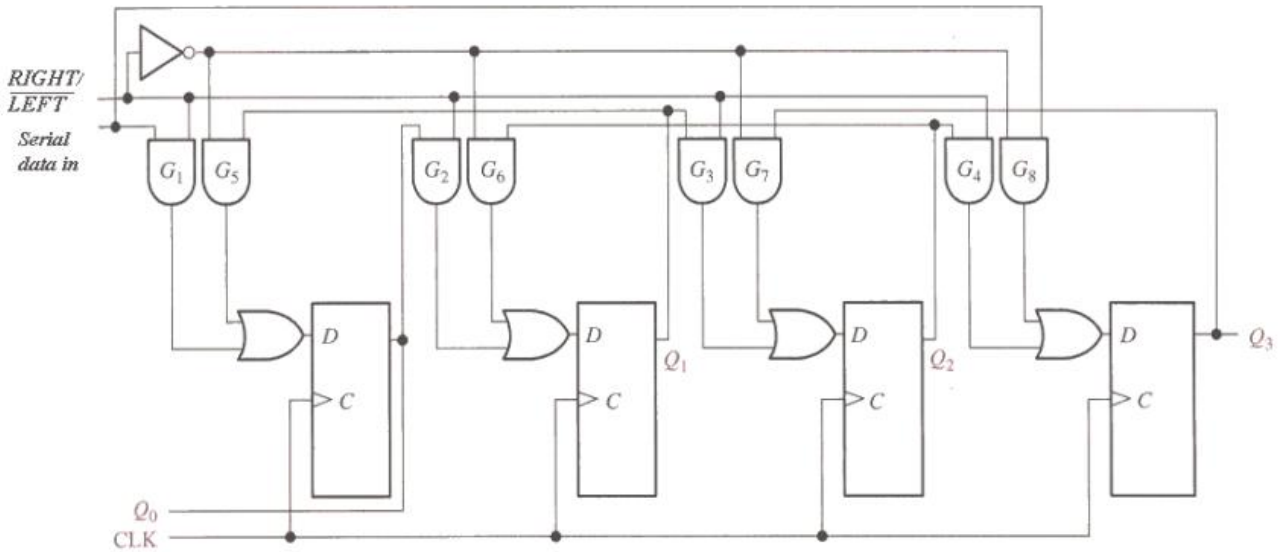


Figure 7.

Shift Register Counters

We have seen that both counters and shift registers are some kinds of cascade arrangement of flip-flops. A shift register, unlike a counter, has no specified sequence of states. However, if the serial output of the shift register is fed back to the serial input, we do get a circuit that exhibits a specified sequence of states. The resulting circuits are known as shift register counters. Depending upon the nature of the feedback, we have two types of shift register counter, namely ther ing counter and the shift counter, also called the Johnson counter. These are briefly described in the following paragraphs.

1- Ring Counter

A ring counter is obtained from a shift register by directly feeding back the true output of the output flip-flop to the data input terminal of the input flip-flop. If Dflip-flops are being used to construct the shift register, the ring counter, also called a circulating register, can be constructed by feeding back the Q output of the output flip-flop back to the D input of the input flip-flop. If J-K flip-flops are being used, the Q and Q outputs of the output flip-flop are respectively fed back to the J and K inputs of the input flip-flop.

Figure 11.45 shows the logic diagram of a four-bit ring counter. Let us assume that flip-flop FF0 is initially set to the logic '1' state and all other flip-flops are reset to the logic '0' state. The counter output is therefore 1000. With the first clock pulse, this '1' gets shifted to the second flip-flop output and the counter output becomes 0100. Similarly, with the second and third clock pulses, the counter output will become 0010 and 0001. With the fourth clock pulse, the counter output will again become 1000. The count cycle repeats in the subsequent clock pulses. Circulating registers of this type find wide application in the control section of microprocessor-based systems where one event should follow the other. The timing waveforms for the circulating register of Figure as shown in Fig. 8, further illustrate their utility as a control element in a digital system to generate control pulses that must occur one after the other sequentially.

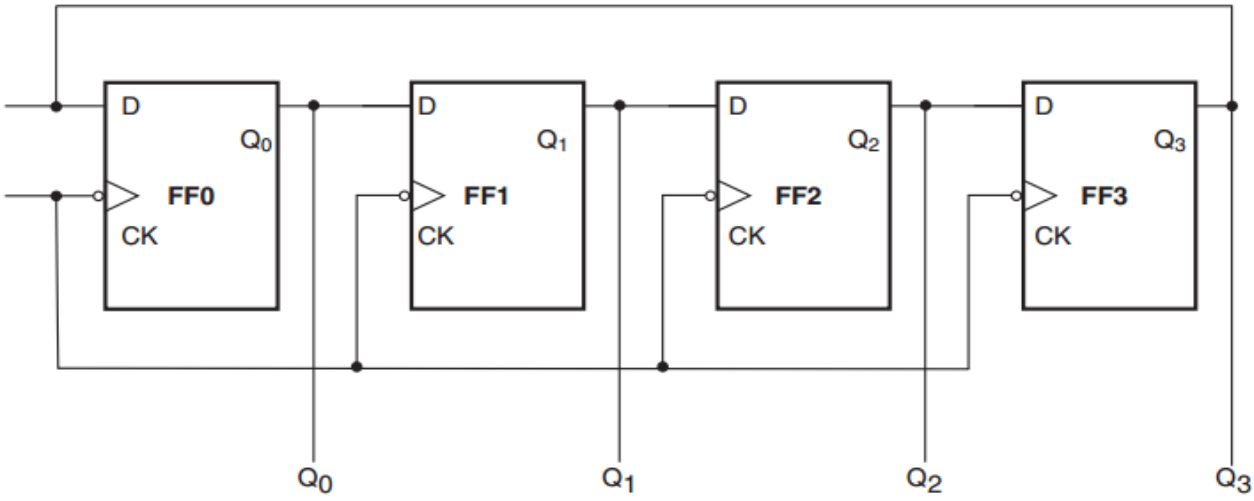
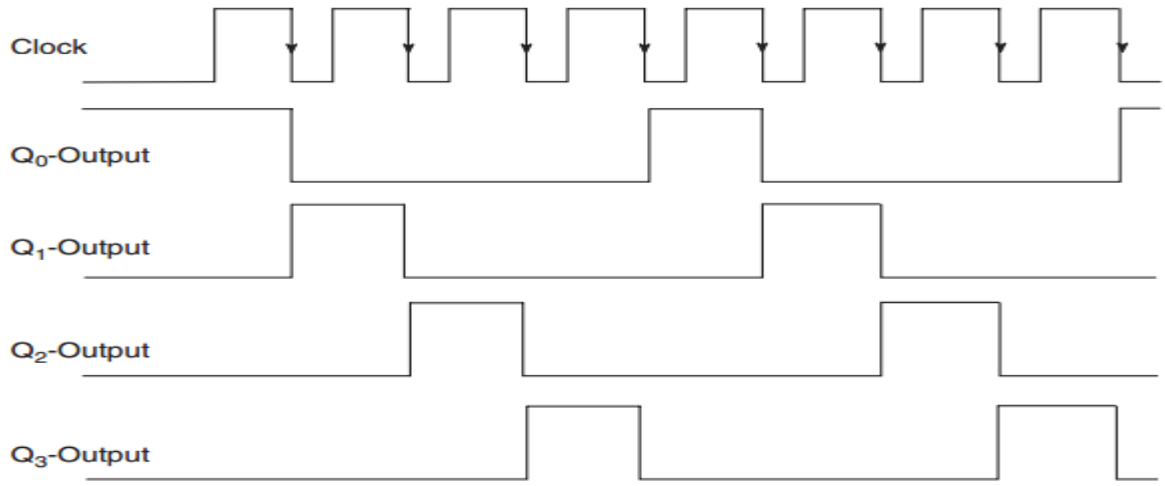


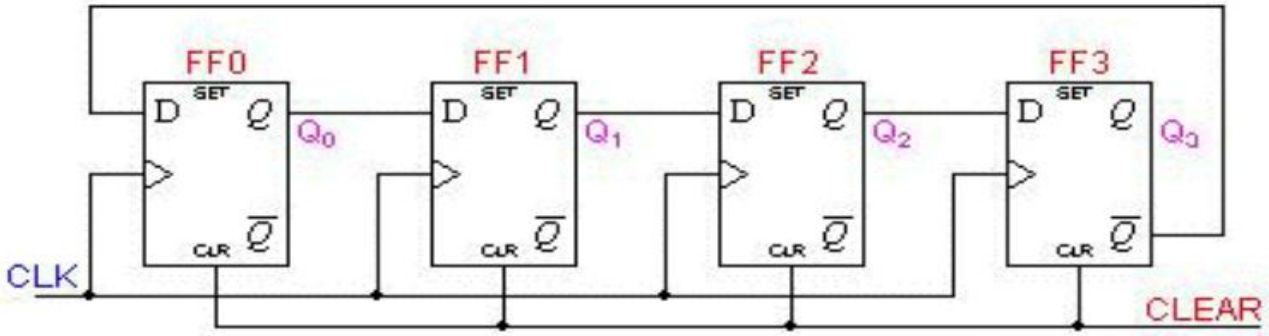
Figure 8. Four-bit ring counter.



Timing waveforms of the four-bit ring counter.

2. Johnson Counters

Johnson counters are a variation of standard ring counters, with the inverted output of the last stage fed back to the input of the first stage. They are also known as twisted ring counters. An n-stage Johnson counter yields a count sequence of length 2n, so it may be considered to be a mod-2n counter. The circuit below shows a 4-bit Johnson counter. The state sequence for the counter is given in the table.



Clock Pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0

- Again, the apparent disadvantage of this counter is that the maximum available states are not fully utilized. Only eight of the sixteen states are being used.

- Beware that for both the Ring and the Johnson counter must initially be forced into a valid state in the count sequence because they operate on a subset of the available number of states. Otherwise, the ideal sequence will not be followed.

Sources:-

1- Fundamentals of Digital Logic and Microcomputer Design.

2- Digital Electronics principles devices and applications.

3- Internet.