Republic of Iraq

The Ministry of Higher Education

& Scientific Research

بسم الله الرحمن الرحيم

University: Diyala
College: Engineering
Department: Computer and S/W
Stage: Third
Lecturer name: ahmed k. jameil
Academic Status: Lecturer
Qualification:master
Place of work: Computer Dept.

Flow up the implementation of course syllabus

Course Instructor	Ahmed K. Jameil				
E_mail	ahmedkhudaer@yahoo.com				
Title	Digital system design				
Course Coordinator					
Course Objective	To provide an in-depth knowledge of the design of digital circuits and the use of Hardware Description Language in digital system design.				
Course Description	To understand different methods used for the simplification of Boolean functions To design and implement combinational circuits To design and implement synchronous sequential circuits To design and implement asynchronous sequential circuits To study the fundamentals of VHDL / Verilog HDL To design and implement Memory To design and implement PLD"s				
Textbook	M.Morris Mano, "Digital Design", ٣rd edition, Pearson Education, ٢٠٠٧.				
Course Assessment	First Term	Mid-Year	٢nd Term	Project	Final Exam
	١٠ %	٢٠ %	١٠ %	----	٦٠ %
General Notes	١. Charles H.Roth, Jr. "Fundamentals of Logic Design", ٤th Edition, Jaico Publishing House, Cengage Earning, ٥th ed, ٢٠٠٥ ٢. Donald D.Givone, "Digital Principles and Design", Tata McGraw-Hill, ٢٠٠٧ ٣. Digital systems VHDL & Verilog design , Dr. mohamed khalil hani, UTM. ٤. CAD for Electronic Design ,lecture notes, Dr. Muhammed Nadzir ,UTM. ٥. Stephen Brown & Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, McGraw-Hill, ٢٠٠٤				

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Course Weekly Outline

week	Date	Topics Covered	Lab. Experiment Assignments	Notes
١	٠٨/١٠/٢٠١٤	Introduction in the digital circuits		
٢	١٥/١٠/٢٠١٤	Rules for planning the digital circuits		
٣	٢٢/١٠/٢٠١٤	Design of combinational Logic circuits		
٤	٢٩/١٠/٢٠١٤	Modeling combinational logic Verilog		
٥	٠٥/١١/٢٠١٤	Modeling sequentail logic in Verilog		
٦	١٢/١١/٢٠١٤	Transistor-Transistor-Logic (T.T.L)		
٧	١٩/١١/٢٠١٤	Test١ ٥٪		
٨	٢٦/١١/٢٠١٤	Complementary metal Oxide Semiconductor		
٩	٠٣/١٢/٢٠١٤	Design of Digital Sequential Circuits		
١٠	١٠/١٢/٢٠١٤	Programmable Logic Array		
١١	١٧/١٢/٢٠١٤	Programmable Array Logic		
١٢	٢٤/١٢/٢٠١٤	Programmable Logic Devices		
١٣	٣١/١٢/٢٠١٤	Test٢ ٥٪		
١٤	٠٦/٠١/٢٠١٥	Holiday		
١٥	--	--		
١٦	--	--		
Half-Year Break				
١٧	١٧/٠٢/٢٠١٥	Design of combinational Circuits using memory Techniques		
١٨	٢٤/٠٢/٢٠١٥	Design of memory circuits		
١٩	٠٣/٠٣/٢٠١٥	Design methods using REED-Muller		
٢٠	١٠/٠٣/٢٠١٥	Test١ ٥٪		
٢١	١٧/٠٣/٢٠١٥	To design and implement synchronous sequential circuits		
٢٢	٢٤/٠٣/٢٠١٥	How logic is controlled		
٢٣	٣١/٠٣/٢٠١٥	Mealy/Moore state machines		

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٢٤	٠٧/٠٤/٢٠١٥	State diagrams & state tables		
٢٥	١٤/٠٤/٢٠١٥	**To design and implement Asynchronous sequential circuits**		
٢٦	٢١/٠٤/٢٠١٥	**Comparison of synchronous/asynchronous circuits**		
٢٧	٢٨/٠٤/٢٠١٥	**Dealing with asynchronous inputs/asynchronous hazards**		
٢٨	٠٥/٠٥/٢٠١٥	To study the fundamental of Races		
٢٩	١٢/٠٥/٢٠١٥	**Algorithm State Machines (A.S.M)**		
٣٠	١٩/٠٥/٢٠١٥	**Finite State Machines (F.S.M)**		
٣١	٢٦/٠٥/٢٠١٥	**Application of Advanced Operational Amplifier circuits**		
٣٢	٠٢/٠٦/٢٠١٥	Test٢ ٥٪		

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Instructor Signature:

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