Chapter 1. Introduction

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

Electronics Revolution

- Age of electronics
  - microcontrollers, DSPs, and other VLSI chips are everywhere
- Electronics of today and tomorrow demand…
  - higher performance (speed) circuits
  - low power circuits for portable applications
  - more mixed signal emphasis
    - wireless hardware
    - high performance signal processing
    - sensors and microsystems

VLSI: Enabling Technology

- Automotive electronic systems
  - A typical Chevrolet has 80 ICs (stereo systems, display panels, fuel injection systems, smart suspensions, antilock brakes, airbags)
- Signal Processing (DSP chips, data acquisition systems)
- Transaction processing (bank ATMs)
- PCs, workstations
- Medical electronics (artificial eye, implants)
- Multimedia

2006 World Semiconductor/VLSI Companies Sales Ranking (wikipedia.org)

Rank 2006	Rank 2005	Company	Country of origin	Revenue (million $ USD)	2006/2005 changes	Market share
1	1	Intel	USA	31 542	-11.1%	12.1%
2	2	Samsung Semiconductors	South Korea	19 842	+12.0%	7.6%
3	3	Texas Instruments	USA	12 600	+17.3%	4.8%
4	4	Toshiba Semiconductors	Japan	10 141	+11.7%	3.9%
5	5	STMicroelectronics	Italy-France	9 854	+11.0%	3.8%
6	7	Renesas Technology (merger of Mitsubishi and Hitachi Semiconductors)	Japan	7 900	-2.6%	3.0%
7	11	Hynix	South Korea	7 865	+41.5%	3.0%
8	15	AMD (1)	USA	7 506	+91.6%	2.9%
9	10	Freescale (3)	USA	5 988	+7.0%	2.3%
10	9	NXP (spin-off from Philips Semiconductors) (2)	Netherlands	5 874	+4.0%	2.3%
11	8	NEC Semiconductors	Japan	5 679	-0.5%	2.2%
12	-	Qimonda (4) (spin-off from Infineon)	Germany	5 413	N/A	2.1%
13	12	Micron Technology	USA	5 210	+9.1%	2.0%
14	6	Infineon (4)	Germany	5 119	-38.3%	2.0%
15	13	Sony	Japan	4 852	+6.1%	1.9%
16	16	Qualcomm	USA	4 529	+31.0%	1.7%
17	14	Matsushita Electric	Japan	4 022	-2.6%	1.5%
18	20	Broadcom	USA	3 668	+37.3	1.4%
19	28	Elpida Memory	Japan	3 527	+98.6%	1.4%
20	17	Sharp Electronics	Japan	3 341	+2.3%	1.3%
21	19	IBM Microelectronics	USA	3 172	+13.6%	1.2%
22	18	Rohm	Japan	2 882	-0.9%	1.1%
23	22	Analog Devices	USA	2 603	+7.2%	1.0%
24	24	Spansion	Japan(63%) and USA(37%) joint venture	2 579	+25.6%	1.0%
25	23	NVIDIA	USA	2 574	+24.4%	1.0%
		Other companies		81 912	+7.3%	31.5%
		TOTAL		260 194	+9.3%	100.0%

A Brief History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2003
  - Intel Pentium 4 µprocessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

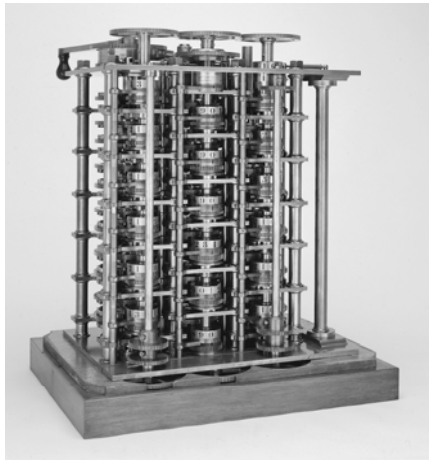
Transistor Revolution

- Transistor –Bardeen (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's

MOSFET Technology

- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI, Copper-Low K, …

The First Computer

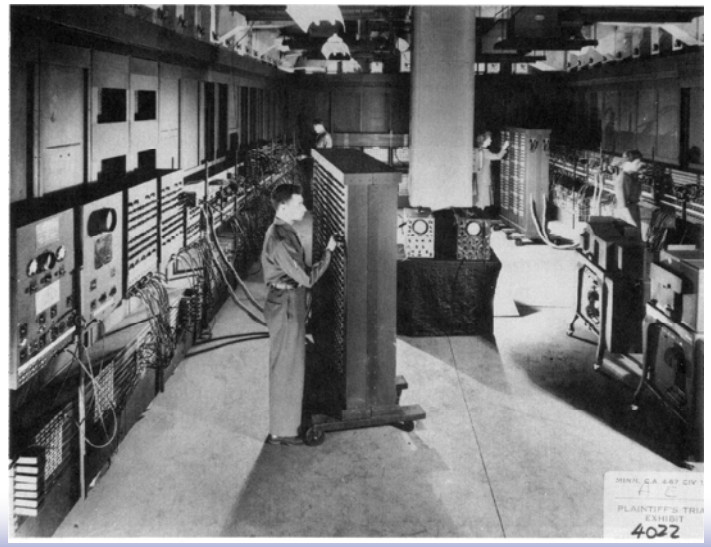


The Babbage Difference Engine (1832)

25,000 parts

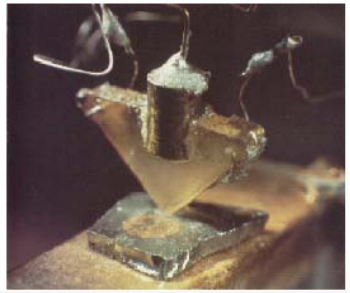
cost: ? 7,470

ENIAC - The first electronic computer (1946)

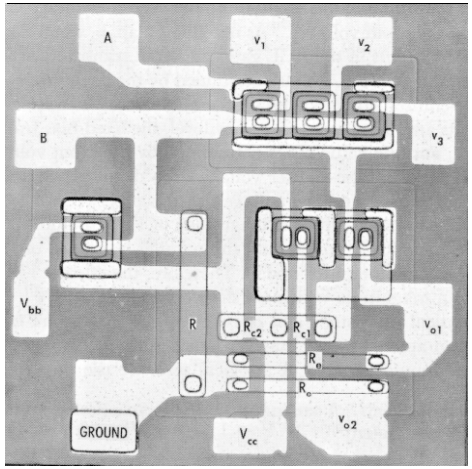


Invention of the Transistor

- Vacuum tubes ruled in first half of 20th century
  Large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
  - John Bardeen and Walter Brattain at Bell Labs
  - Read *Crystal Fire*
    by Riordan, Hoddeson



The First Integrated Circuits

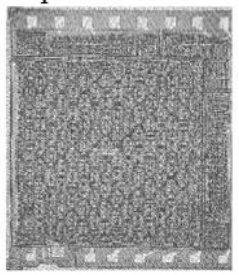


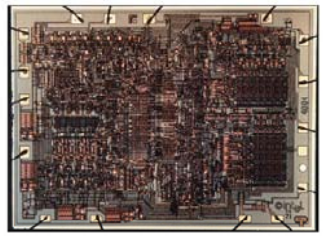
Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

MOS Integrated Circuits

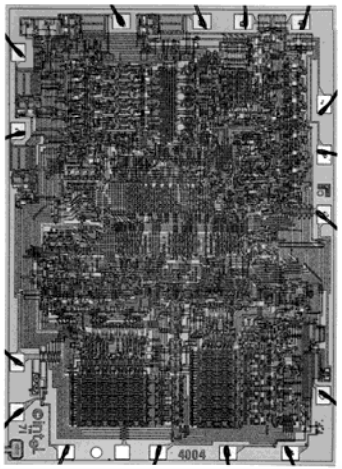
- 1970's processes usually had only nMOS transistors
  - Inexpensive, but consume power while idle
  - 1980s-present: CMOS processes for low idle power





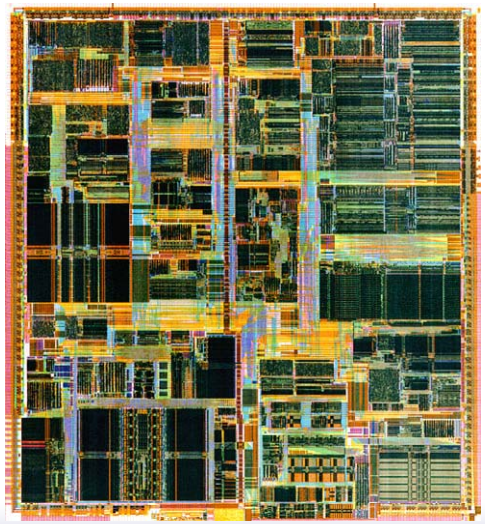
Intel 1101 256-bit SRAM Intel 4004 4-bit μProc

Intel 4004 Micro-Processor

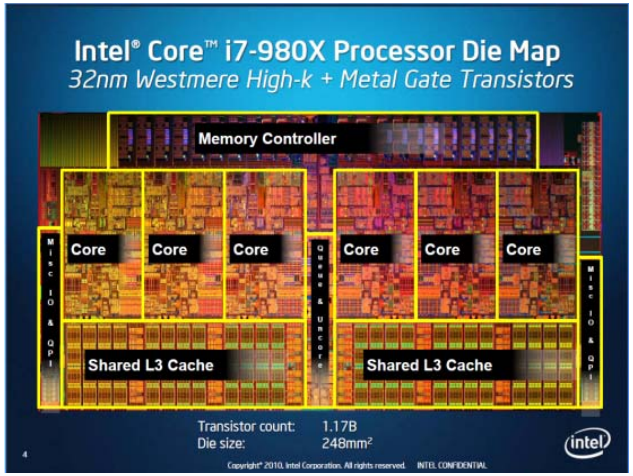


1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



Intel Core i7-980X Processor



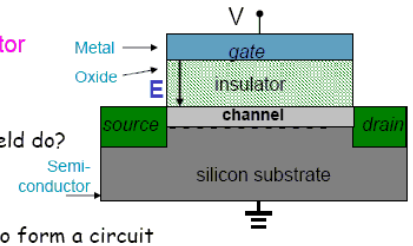
VLSI Technology

- CMOS: Complementary Metal Oxide Silicon
  - Based on voltage-controlled field-effect transistors (FETs)
- Other technologies: bipolar junction transistors (BJTs), BiCMOS, gallium arsenide (GaAs)
  - BJTs, BiCMOS, ECL circuits are faster but CMOS consumes lower power and are easier to fabricate
  - GaAs carriers have higher mobility but high integration levels are difficult to achieve in GaAs technology

- CMOS dominates the semiconductor/IC industry
  - **Silicon is cheaper** → preferred over other materials
  - **physics** of CMOS is **easier** to understand
  - CMOS is **easier to implement/fabricate**
  - CMOS provides **lower power-delay product**
  - CMOS is **lowest power**
  - density: can get **more** CMOS transistors/functions **in same chip area**
- **BUT!** CMOS is not the fastest technology!
  - BJT and III-V devices are faster

What is a MOSFET?

- Digital integrated circuits rely on transistor switches
  - most common device for digital and mixed signal: MOSFET
- Definitions
  - MOS = Metal Oxide Semiconductor
    - physical layers of the device
  - FET = Field Effect Transistor
    - What field? What does the field do?
    - Are other fields important?
  - CMOS = Complementary MOS
    - use of both nMOS and pMOS to form a circuit

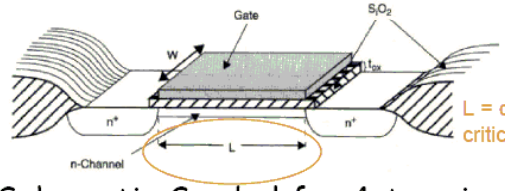


- Primary Features
  - gate
  - gate oxide (insulator)
  - source and drain
  - bulk/substrate
  - channel

NOTE: "metal" is replaced by polysilicon in modern MOSFETs

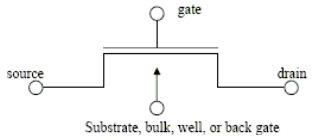
MOSFET Physical View

- Phvsical Structure of a MOSFET Device

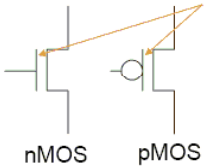


L = channel length
critical dimension = "feature size"

- Schematic Symbol for 4-terminal MOSFET



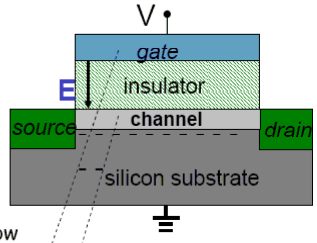
- Simplified Symbols



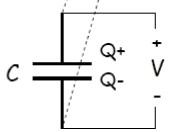
note: no physical connection at Gate terminal, symbolic of gate insulator in MOSFET

Fundamental Relations in MOSFET

- Electric Fields
  - fundamental equation
    - electric field: E = V/d
  - vertical field through gate oxide
    - determines charge induced in channel
  - horizontal field across channel
    - determines source-to-drain current flow



- Capacitance
  - fundamental equations
    - capacitor charge: Q = CV
    - capacitance: C = ε A/d
  - charge balance on capacitor, Q+ = Q-
    - charge on gate is balanced by charge in channel
    - what is the source of channel charge? where does it come from?



CMOS Cross Section View

- Cross section of a 2 metal, 1 poly CMOS process

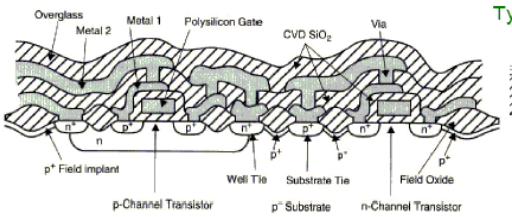
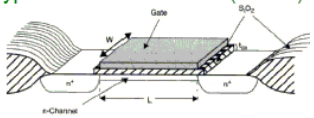
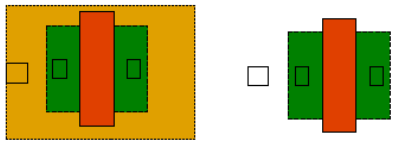


Figure 2.11 The final cross section of a CMOS microcircuit with two layers of metal.

Typical MOSFET Device (nMOS)

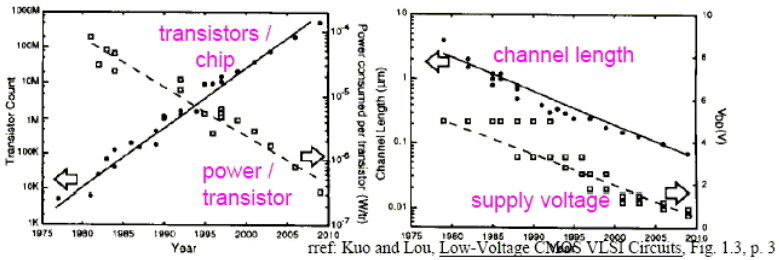


- Layout (top view) of the devices above (partial, simplified)



CMOS Technology Trends

- Variations over time
  - # transistors / chip: increasing with time
  - power / transistor: decreasing with time (constant power density)
  - device channel length: decreasing with time
  - power supply voltage: decreasing with time



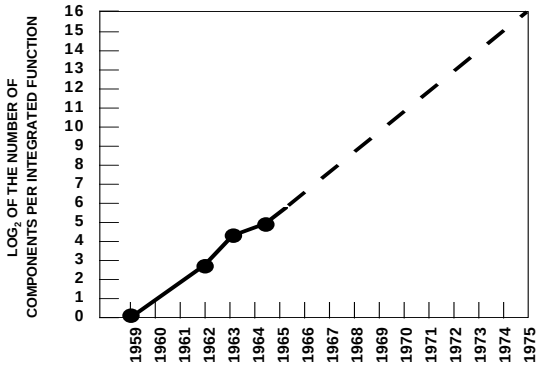
ref: Kuo and Lou, Low-Voltage CMOS VLSI Circuits, Fig. 1.3, p. 3

low power/voltage is critical for future ICs

Moore's Law

- In 1965, Gordon Moore predicted that the number of transistors that can be integrated on a die would double every 18 to 14 months (i.e., grow exponentially with time).
- Amazingly visionary – million transistor/chip barrier was crossed in the 1980's.
  - 2300 transistors, 1 MHz clock (Intel 4004) - 1971
  - 16 Million transistors (Ultra Sparc III)
  - 42 Million, 2 GHz clock (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

Moore's Law

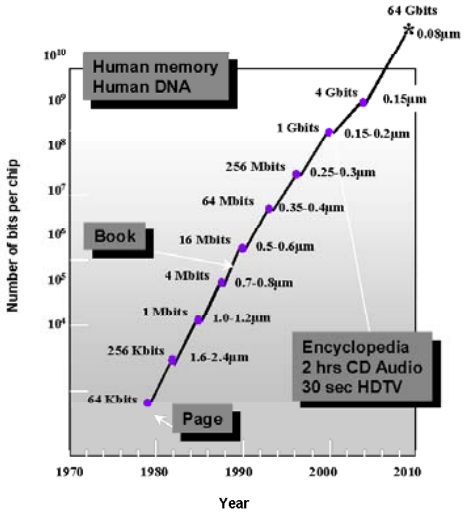


Electronics, April 19, 1965.

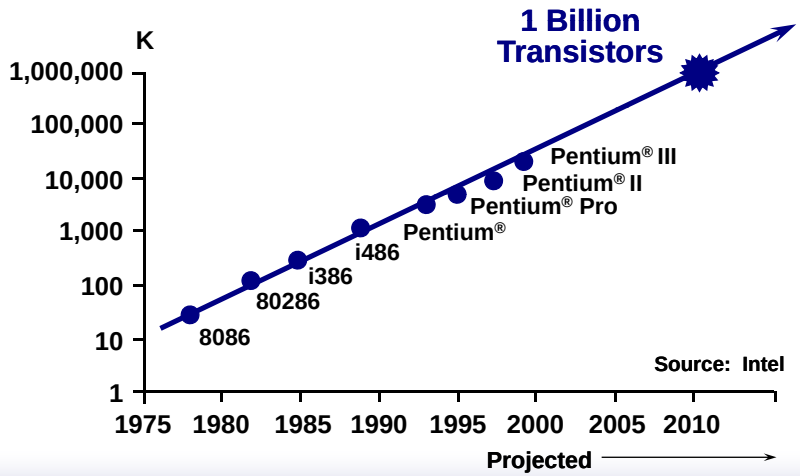
State-of-the Art: Lead Microprocessors

Processor	Alpha 21264B	AMD Athlon	HP PA-8600	IBM Power3-II	Intel Pentium III	Intel Pentium 4	MIPS R12000	Sun Ultra-II	Sun Ultra-III
Clock Rate	833MHz	1.33GHz	552MHz	450MHz	1.0GHz	1.7GHz	400MHz	480MHz	900MHz
Cache (I/D/L2)	64K/64K	64K/64K/256K	512K/1M	32K/64K	16K/16K/256K	12K/8K/256K	32K/32K	16K/16K	32K/64K
Issue Rate	4 issue	3 x86 instr	4 issue	4 issue	3 x86 instr	3 ROPs	4 issue	4 issue	4 issue
Pipeline Stages	7/9 stages	9/11 stages	7/9 stages	7/8 stages	12/14 stages	22/24 stages	6 stages	6/9 stages	14/15 stages
Out of Order	80 instr	72ROPs	56 instr	32 instr	40 ROPs	126 ROPs	48 instr	None	None
Rename regs	48/41	36/36	56 total	16 int/24 fp	40 total	128 total	32/32	None	None
BHT Entries	4K x 9 bits	4K x 2 bits	2K x 2 bits	2K x 2 bits	≥ 512	4K x 2 bits	2K x 2 bits	512 x 2 bits	16K x 2 bits
TLB Entries	128/128	280/288	120 unified	128/128	32I/64D	128I/64D	64 unified	64I/64D	128I/512D
Memory B/W	2.66GB/s	2.1GB/s	1.54GB/s	1.6GB/s	1.06GB/s	3.2GB/s	539 MB/s	1.9GB/s	4.8GB/s
Package	CPGA-588	PGA-462	LGA-544	SCC-1088	PGA-370	PGA-423	CPGA-527	CLGA-787	1368 FC-LGA
IC Process	0.18μ 6M	0.18μ 6M	0.25μ 2M	0.22μ 6M	0.18μ 6M	0.18μ 6M	0.25μ 4M	0.29μ 6M	0.18μ 7M
Die Size	115mm²	117mm²	477mm²	163mm²	106mm²	217mm²	204mm²	126mm²	210mm²
Transistors	15.4 million	37 million	130 million	23 million	24 million	42 million	7.2 million	3.8 million	29 million
Est mfg cost	$160	$62	$330	$110	$39	$100	$125	$70	$145
Power (max)	75W*	76W	60W*	36W*	30W	64W(TDP)	25W*	20W*	65W
Availability	1Q01	1Q01	3Q00	4Q00	2Q00	2Q01	2Q00	3Q0	4Q00

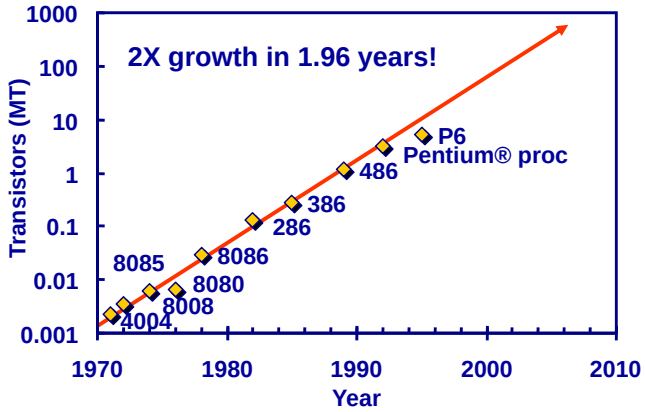
Evolution in Complexity



Transistor Counts

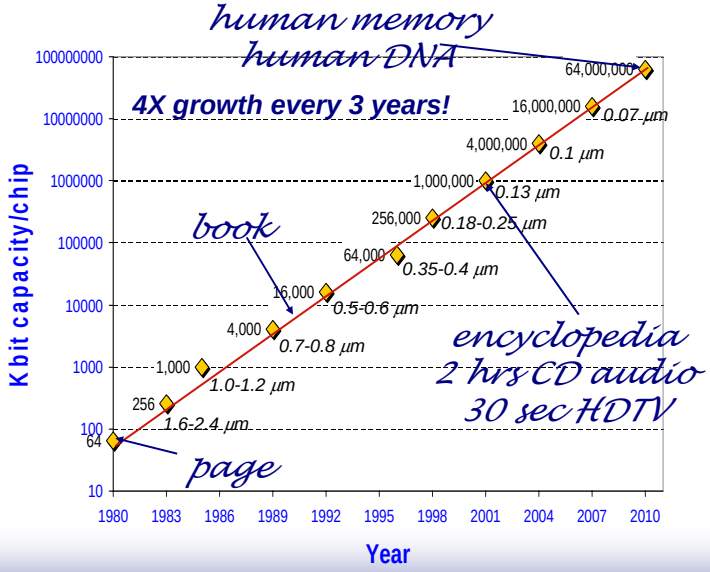


Moore's law in Microprocessors

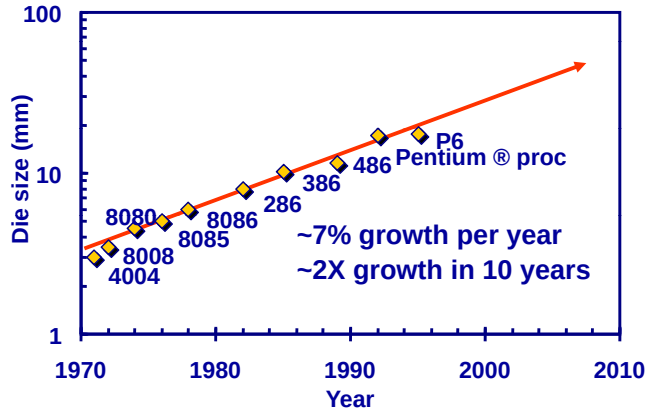


Transistors on Lead Microprocessors double every 2 years

Evolution in DRAM Chip Capacity

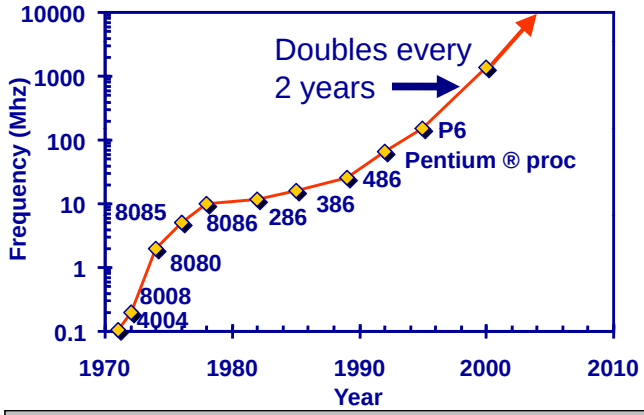


Die Size Growth



Die size grows by 14% to satisfy Moore's Law

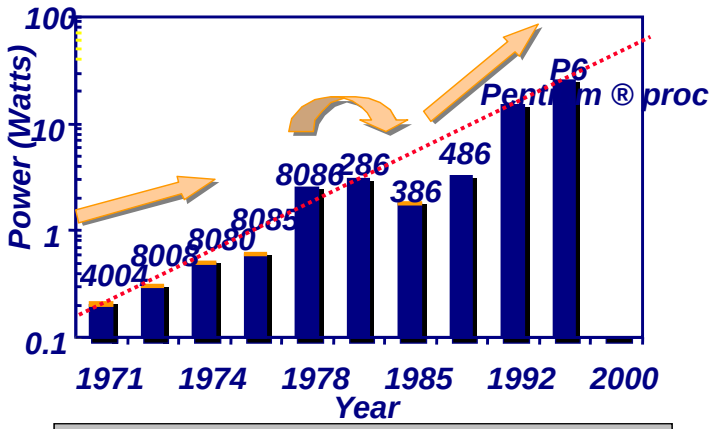
Clock Frequency



Lead Microprocessors frequency doubles every 2 years

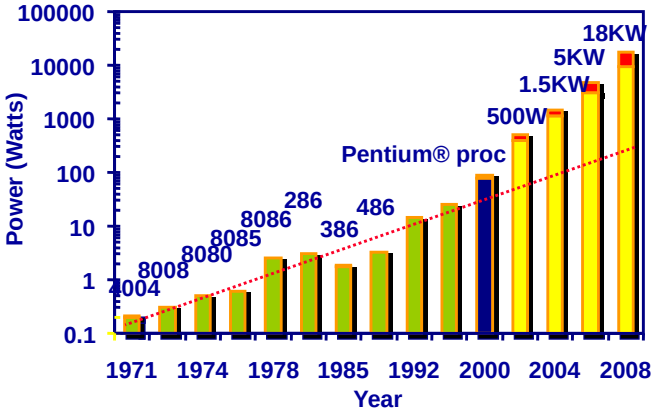
Power Dissipation

Lead Microprocessors power continues to increase



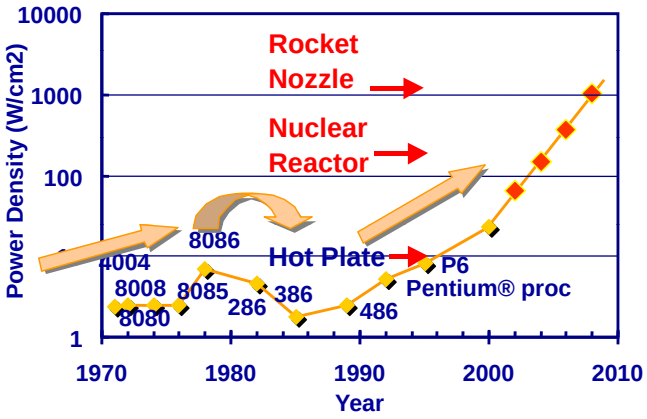
Power delivery and dissipation will be prohibitive

Power will be a major problem



Power delivery and dissipation will be prohibitive

Power density



Power density too high to keep junctions at low temp

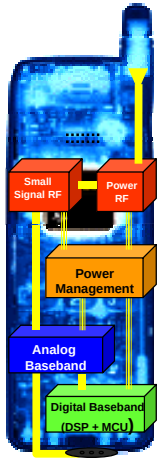
Not Only Microprocessors

Cell Phone

Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Technology Directions: SIA Roadmap

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Mtrans/cm^2	7	14-26	47	115	284	701
Chip size (mm^2)	170	170-214	235	269	308	354
Signal pins/chip	768	1024	1024	1280	1408	1472
Clock rate (MHz)	600	800	1100	1400	1800	2200
Wiring levels	6-7	7-8	8-9	9	9-10	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.6
High-perf power (W)	90	130	160	170	174	183
Battery power (W)	1.4	2.0	2.4	2.0	2.2	2.4

For Cost-Performance MPU (L1 on-chip SRAM cache; 32KB/1999 doubling every two years)

http://www.itrs.net/ntrs/publntrs.nsf

What is this course all about?

- **Introduction to digital integrated circuits.**
  - CMOS devices and manufacturing technology. CMOS inverters and gates. Propagation delay, noise margins, and power dissipation. Sequential circuits. Arithmetic, interconnect, and memories. Programmable logic arrays. Design methodologies.
- **What will you learn?**
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability

Digital Integrated Circuits

- Introduction: Issues in digital design
- The CMOS inverter
- Combinational logic structures
- Sequential logic gates
- Design methodologies
- Interconnect: R, L and C
- Timing
- Arithmetic building blocks
- Memories and array structures

Challenges in Digital Design

- *Why is designing digital ICs different today than it was before?*
- *Will it change in future?*

∝ DSM

"Microscopic Problems"

- **Ultra-high speed design**
- **Interconnect**
- **Noise, Crosstalk**
- **Reliability, Manufacturability**
- **Power Dissipation and supply rail drop**
- **Clock distribution.**

Everything Looks a Little Different

?

∝ 1/DSM

"Macroscopic Issues"

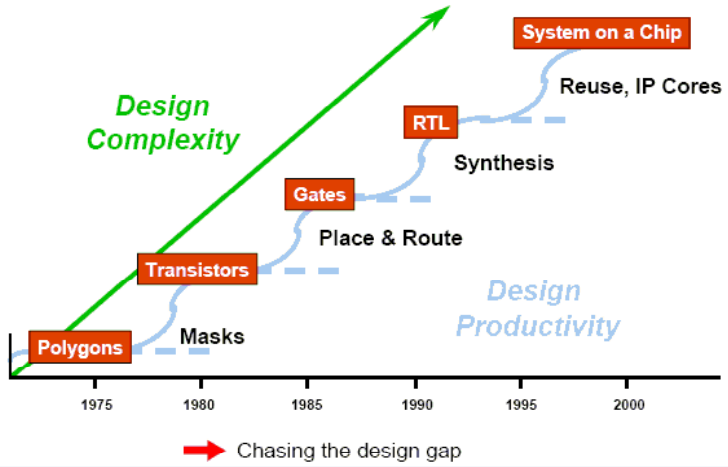
- **Time-to-Market**
- **Design complexity: Millions of Gates**
- **High-Level Abstractions**
- **Design for testability**
- **Reuse & IP, Portability**
- **System on a chip (SoC)**
- **Predictability**
- **Tool interoperability**

…and There's a Lot of Them!

New Design Challenges

- Interconnect-centric design
  - Capacitive coupling, inductance effects, delay modeling
- Power densities, power grid design, leakage
  - 80 W/cm^2 ~ 100 W/cm^2
    - Nuclear reactor: 150 W/cm^2
  - 80% increase in power density per generation (voltage scales by 0.8)
  - 225% increase in current density
  - 1.3V power supply leads to 60W power with 60A sustained current
    - 2X the current (surge) in your car's alternator
- Statistical design (P,V,T)

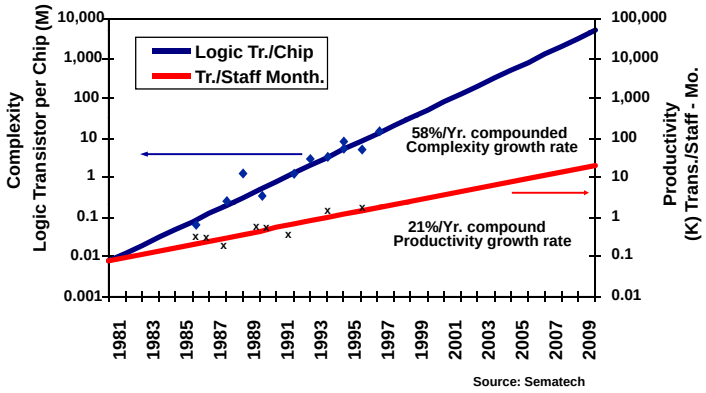
Challenge: System-on-a-Chip Design ?



Challenges in Digital Design

- Digital integrated circuits experience exponential growth in complexity (Moore's law) and performance
- Design in the deep submicron (DSM) era creates new challenges
  - Devices become somewhat different
  - Global clocking becomes more challenging
  - Interconnect effects play a more significant role
  - Power dissipation may be *the* limiting factor

Design Productivity Trends

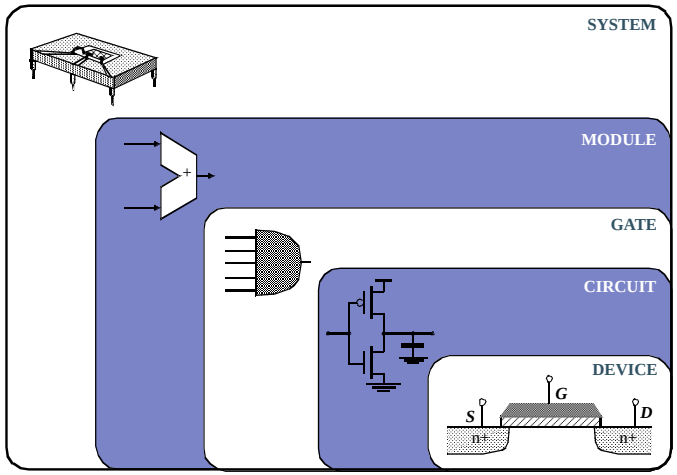


Complexity outpaces design productivity

Why Scaling?

- Technology shrinks by ~0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels

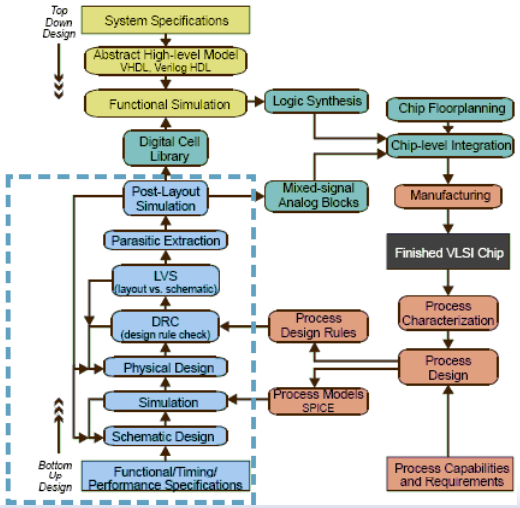


VLSI Design Flow

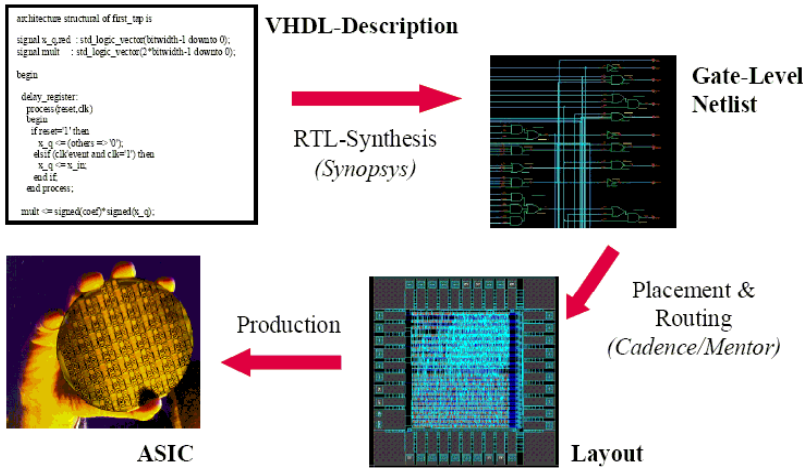
VLSI = very large scale integration
- lots of transistors integrated on a single chip

Design Methodologies

- Top Down Design
  - coded circuit functionality for rapid design
  - digital only
- Bottom Up Design
  - transistor-level design with focus on circuit performance
  - digital & mixed signal



EDA: High-Level Design



Design Metrics

How to evaluate performance of a digital circuit (gate, block, …)?

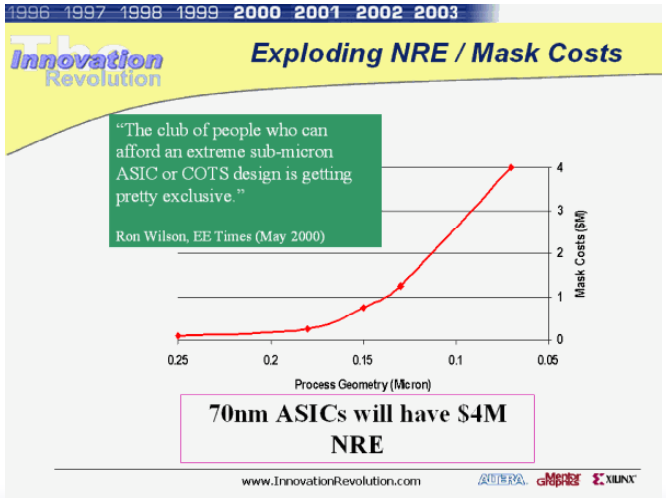
- Functionality
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay, operating frequency)
  - Power consumption; energy to perform a function
- Time-to-market

Cost of Integrated Circuits

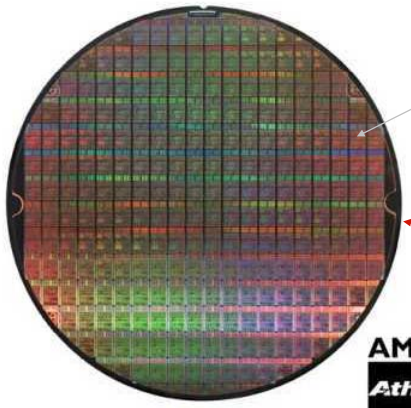
- NRE (non-recurring engineering) costs: one time cost factor
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume and chip area
  - silicon processing
    - also proportional to chip area
  - assembly (packaging)
  - test

$$\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}$$

NRE Cost is Increasing



Die Cost

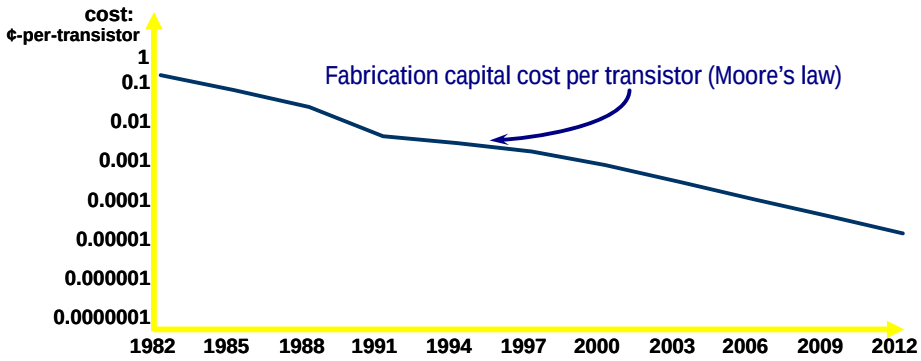


AMD Athlon

Going up to 12″ (30cm)

From http://www.amd.com

Cost per Transistor



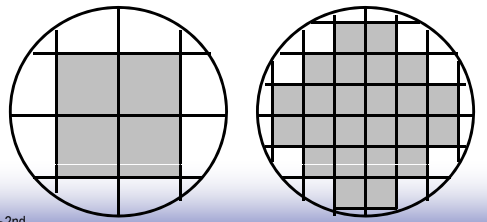
Recurring Costs

$$\text{variable cost} = \frac{\text{cost of die + cost of die test + cost of packaging}}{\text{final test yield}}$$

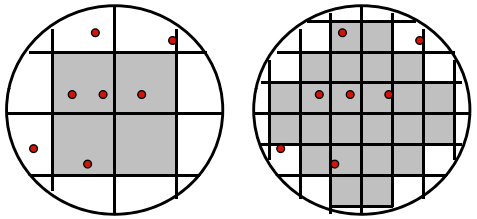
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Yield Example

- *Example*
  - *wafer size of 12 inches, die size of 2.5 cm^2, 1 defects/cm^2, $\alpha = 3$ (measure of manufacturing process complexity)*
  - *252 dies/wafer (remember, wafers round & dies square)*
  - *die yield of 16%*
  - *252 x 16% = only 40 dies/wafer die yield !*
- *Die cost is strong function of die area*
  - *proportional to the third or fourth power of the die area*

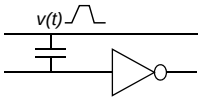
Examples of Cost Metrics (1994)

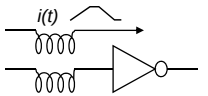
Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability

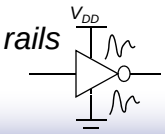
Noise in Digital Integrated Circuits

- Noise – unwanted variations of voltages and currents at the logic nodes
- *from two wires placed side by side*
  - *capacitive coupling*
    - *voltage change on one wire can influence signal on the neighboring wire*
    - *cross talk*
  - *inductive coupling*
    - *current change on one wire can influence signal on the neighboring wire*





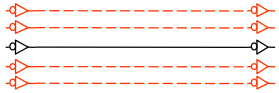
- *from noise on the power and ground supply rails*
  - *can influence signal levels in the gate*



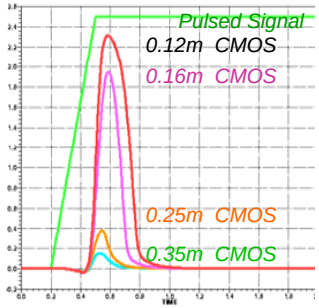
Example of Capacitive Coupling

- Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

Crosstalk vs. Technology



Black line quiet
Red lines pulsed
Glitches strength vs technology



From Dunlop, Lucent, 2000

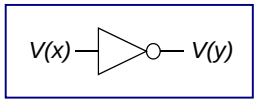
Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables

$$x \in \{0,1\}$$

- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



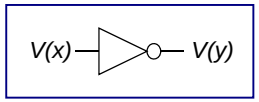
$V_{OH} = !\,(V_{OL})$
$V_{OL} = !\,(V_{OH})$

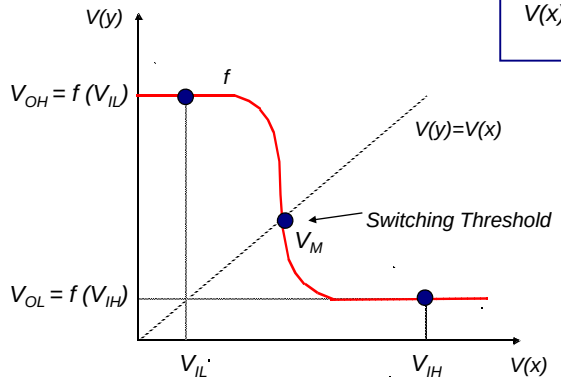
- *Difference between V_{OH} and V_{OL} is the logic or signal swing V_{sw}*

DC Operation

Voltage Transfer Characteristics (VTC)

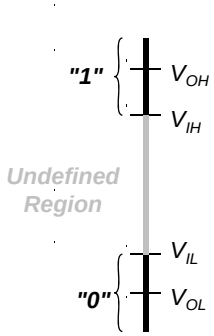
- *Plot of output voltage as a function of the input voltage*

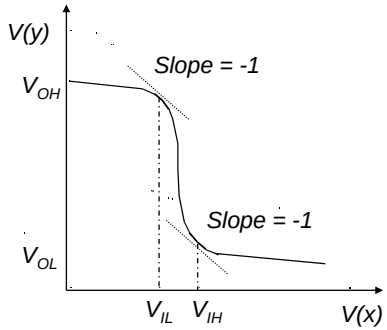




Mapping Logic Levels to the Voltage Domain

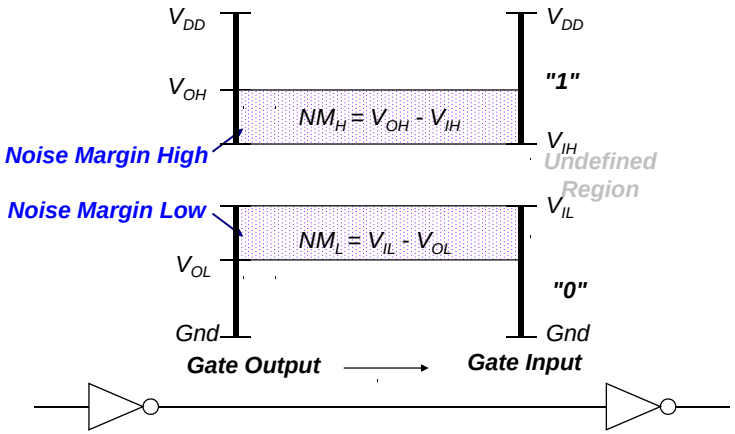
- *The regions of acceptable high and low voltages are delimited by V_{IH} and V_{IL} that represent the points on the VTC curve where the gain = -1*





Noise Margins

- *For robust circuits, want the "0" and "1" intervals to be a s large as possible*



- *Large noise margins are desirable, but not sufficient …*

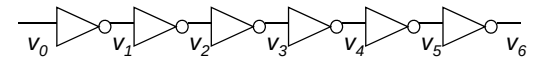
Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources

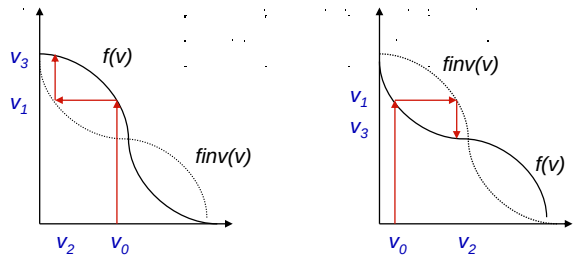
Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

Conditions for Regeneration



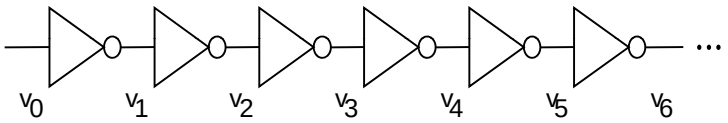
$v_1 = f(v_0) \Rightarrow v_1 = finv(v_2)$



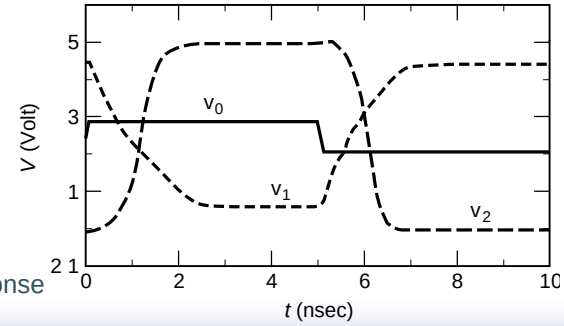
Regenerative Gate *Nonregenerative Gate*

- *To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.*

Regenerative Property



A chain of inverters



Simulated response

Noise Immunity

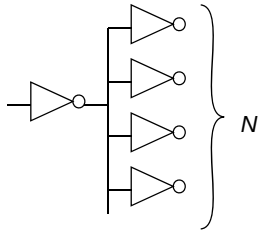
- *Noise margin expresses the ability of a circuit to overpower a noise source*
  - *noise sources: supply noise, cross talk, interference, offset*
- *Absolute noise margin values are deceptive*
  - *a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)*
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

Directivity

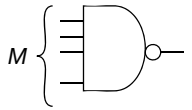
- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)
- Key metrics: *output impedance* of the driver and *input impedance* of the receiver
  - ideally, the output impedance of the driver should be zero
  - input impedance of the receiver should be infinity

Fan-In and Fan-Out

- *Fan-out – number of load gates connected to the output of the driving gate*
  - *gates with large fan-out are slower*

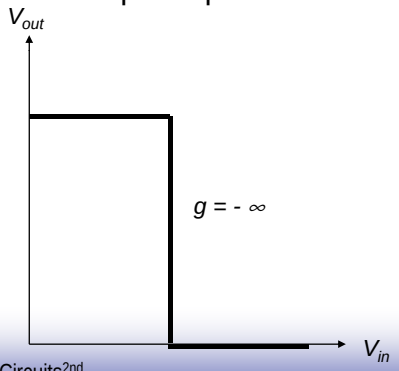


- *Fan-in – the number of inputs to the gate*
  - *gates with large fan-in are bigger and slower*



The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



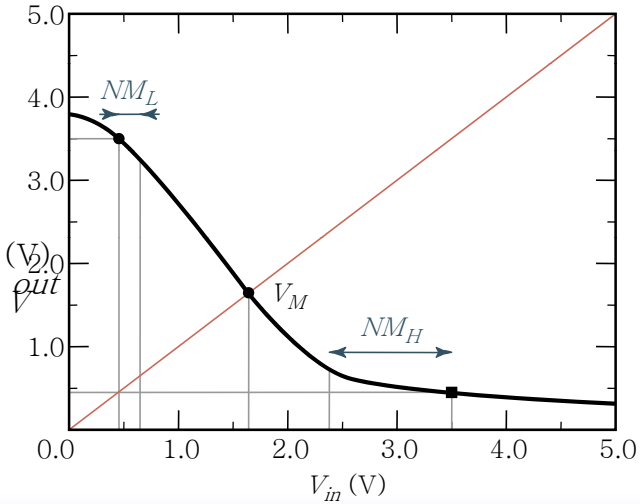
$R_i = \infty$

$R_o = 0$

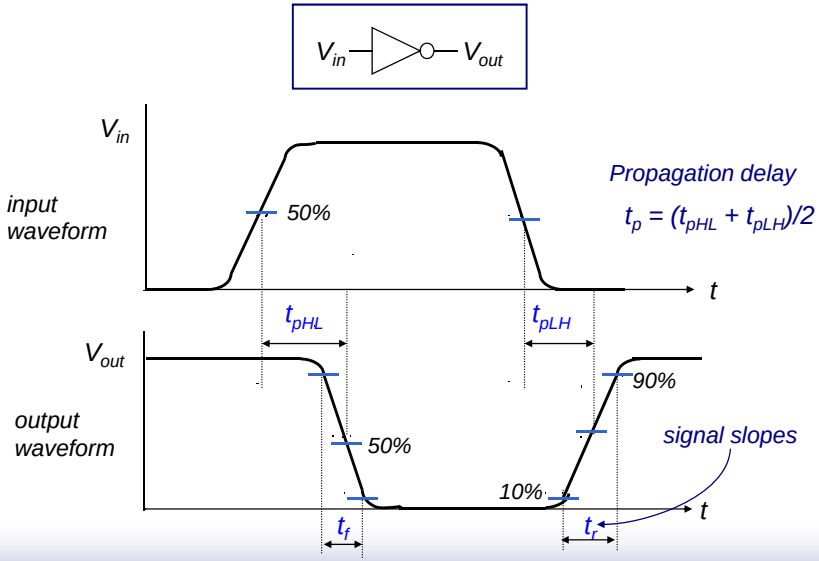
$Fanout = \infty$

$NM_H = NM_L = VDD/2$

An Old-time Inverter



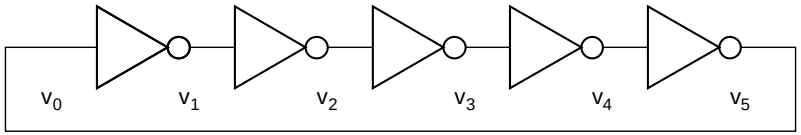
Delay Definitions

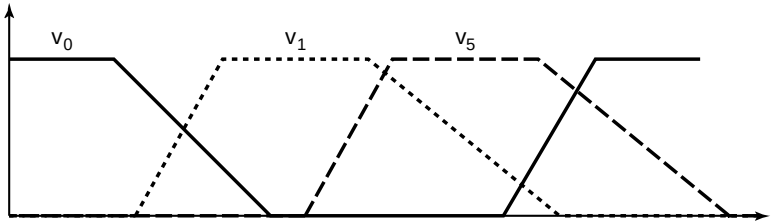


Propagation delay

$t_p = (t_{pHL} + t_{pLH})/2$

Ring Oscillator Circuit

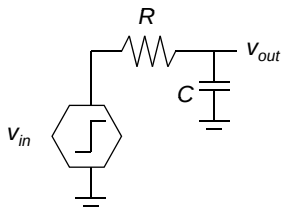




$$T = 2 \times t_p \times N$$

Modeling Propagation Delay

- Model circuit as first-order RC network



$v_{out}(t) = (1 - e^{-t/\tau})V$

where $\tau = RC$

Time to reach 50% point is
$t = \ln(2)\ \tau = 0.69\ \tau$

Time to reach 90% point is
$t = \ln(9)\ \tau = 2.2\ \tau$

- *Matches the delay of an inverter gate*

Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
  - supply line sizing (determined by peak power)
    $P_{peak} = V_{dd} i_{peak}$
  - battery lifetime (determined by average power dissipation)
    $p(t) = v(t)i(t) = V_{dd} i(t)$ $\quad P_{avg} = 1/T \int p(t)\,dt = V_{dd}/T \int i_{dd}(t)\,dt$
  - packaging and cooling requirements
- Two important components: static and dynamic

$$E\ (joules) = C_L V_{dd}^2 P_{0\to1} + t_{sc} V_{dd} I_{peak} P_{0\to1} + V_{dd} I_{leakage}$$

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P\ (watts) = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply} i(t)$$

Peak power:

$$P_{peak} = V_{supply} i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- *For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant*
  - *Power-delay product (PDP) – energy consumed by the gate per switching event*
- *An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is*
  - *Energy-delay product (EDP) = power-delay ^{2}*

Energy and Energy-Delay

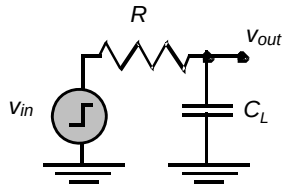
Power-Delay Product (PDP) =

E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

A First-Order RC Network



$$E_{0\to 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this course
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation