Chapter 4. The Wire

[Adapted from Rabaey's *Digital Integrated Circuits*, ©2002, J. Rabaey et al.]

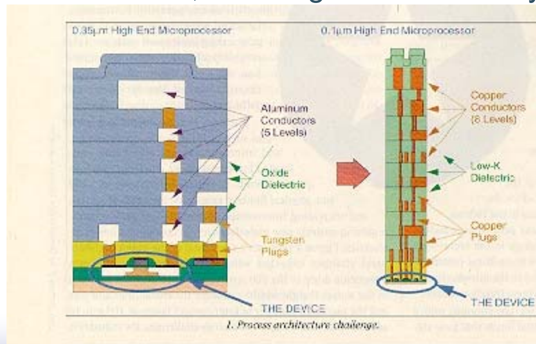
The Wire

- As VLSI technology enters deep submicron and nanometer era, wires start to dominate transistors in affecting the relevant metrics (speed, energy consumption, reliability) of VLSI circuits.

PowerPC Metal Layers

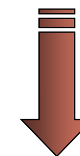
Interconnect Impact on Chip

- Parasitic effects (capacitive, resistive, inductive) of wires result in multiple effects on circuit behavior:
- ✓ Increase propagation delay: performance degradation
- ✓ Affecting energy/power dissipation
- ✓ Introduce extra noises, affecting circuit reliability



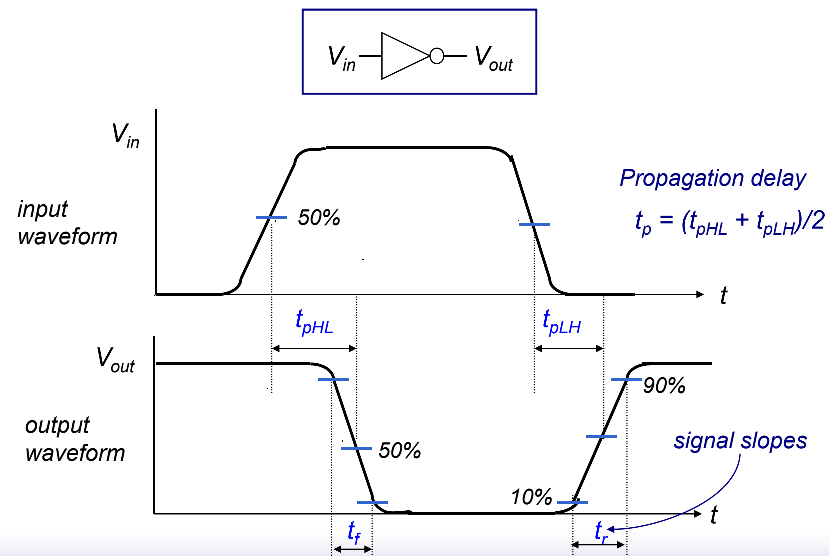
Impact of Interconnect Parasitics

- Interconnect parasitics
  - reduce reliability
  - affect performance and power consumption
- Classes of parasitics
  - Capacitive
  - Resistive
  - Inductive



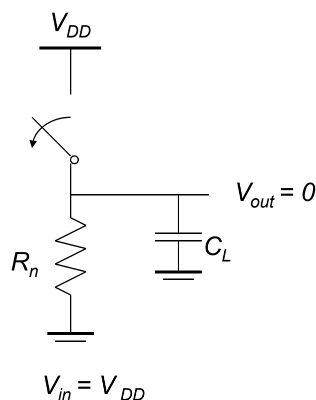
INTERCONNECT

Review: Delay Definitions



CMOS Inverter: Dynamic

- *Transient, or dynamic, response determines the maximum speed at which a device can be operated.*

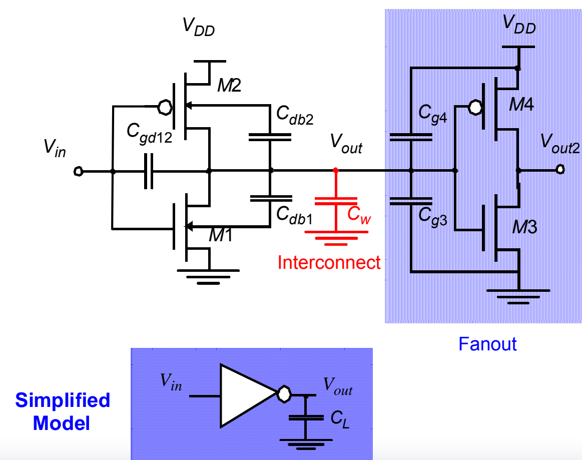


Today's focus

$t_{pHL} = f(R_n, C_L)$

Next lecture's focus

Capacitance of Wire Interconnect

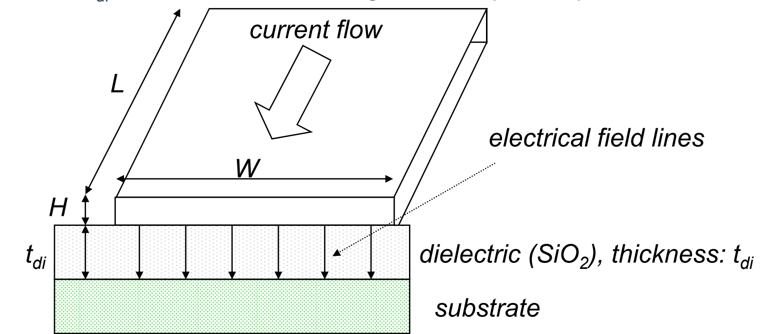


Wiring Capacitance

- The wiring capacitance depends upon the length and width of the connecting wires and is a function of the fan-out from the driving gate and the number of fan-out gates.
- Wiring capacitance is growing in importance with the scaling of technology.

Capacitance: The Parallel Plate Model

- Capacitance of a simple rectangle wire (width: W, length: L) placed above Si substrate: parallel-plate capacitance model. Assume W>>t_{di}, E-field lines are orthogonal to capacitor plates.



$$C_{int} = \frac{\varepsilon_r \varepsilon_0}{t_{di}} WL \qquad S_{Cwire} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

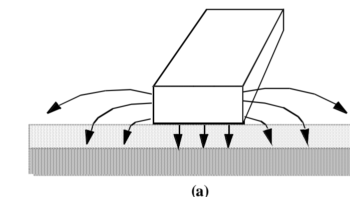
ε_r: Relative permittivity constant (ε_{r_SiO2}= 3.9), ε_0=8.85×10^{-12}F/m

Permittivity Values of Some Dielectrics

Material	ε_r
Free space	1
Aerogels	~1.5
Aromatic thermosets (SiLK)	2.6 – 2.8
Polyimides (organic)	3 – 4
Fluorosilicate glass (FSG)	3.2 – 4.0
Silicon dioxide (SiO_2)	3.9
Glass epoxy (PCBs)	5
Silicon nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance

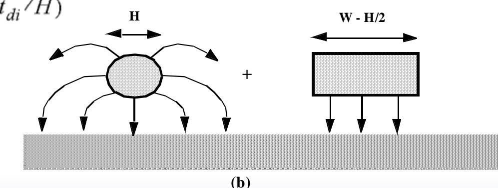
- Wire width (W) has been reduced for denser wiring and less area overhead. If W/H<1, fringing capacitance (capacitance between sidewalls of wires and substrate) must be considered.
- Wire capacitance c_{wire} per unit length considering fringing capacitance:



(a)

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(2t_{di}/H)}$$

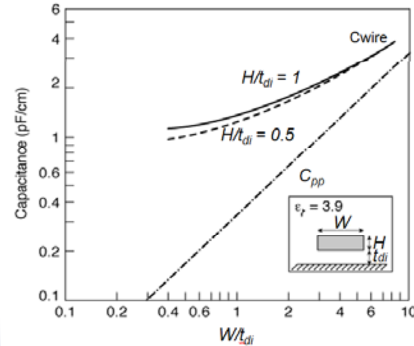
Where: w=(W-H/2).



(b)

Impact of Fringe Capacitance

- When W/t_{di} is large, c_{wire} approaches parallel-plate model.
- For $W/t_{di}<1.5$, c_{fringe} becomes dominant component.
- For very small W/t_{di}, $c_{wire} \rightarrow 1pF/cm$ (constant, no longer a function of wire width W)

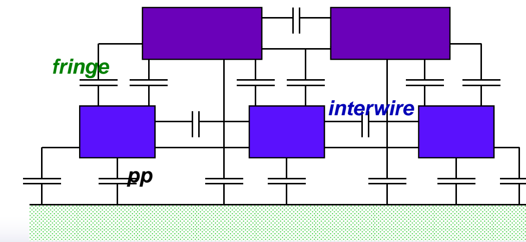


(from [Bakoglu89])

Sources of Interwire Capacitance

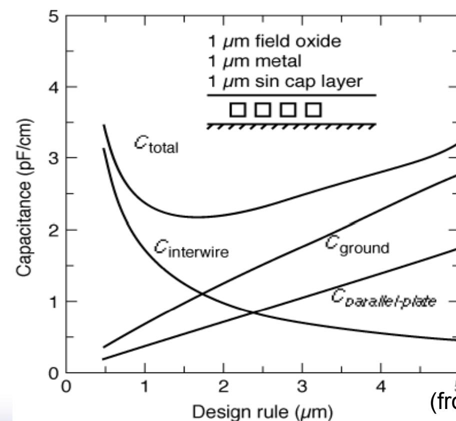
- Actual VLSI: multilayer interconnect. Each wire is not only coupled to gnd, but also to neighboring wires on the same and adjacent layers.
- Interwire floating capacitors lead to noises and performance degradation.

$$C_{wire} = C_{pp} + C_{fringe} + C_{interwire} = (\varepsilon_{di}/t_{di})WL + (2\pi\varepsilon_{di})L/\log(2t_{di}/H+1) + (\varepsilon_{di}/gap)HL_{ov}$$



Impact of Interwire Capacitance

- Interwire capacitance has increasing contribution to the total capacitance with decreasing feature sizes.



(from [Bakoglu89])

Insights

- For W/H < 1.5, the fringe component dominates the parallel-plate component. Fringing capacitance can increase the overall capacitance by a factor of 10 or more.
- When W < 1.75H interwire capacitance starts to dominate
- Interwire capacitance is more pronounced for wires in the higher interconnect layers (further from the substrate)
- Rules of thumb
  - Never run wires in diffusion
  - Use poly only for short runs
  - Shorter wires – lower R and C
  - Thinner wires – lower C but higher R
- Wire delay nearly proportional to L^2

Wiring Capacitances

Non-shaded: C_{pp} in aF/μm^2
Shaded: C_{fringe} in aF/μm

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

	Poly	Al1	Al2	Al3	Al4	Al5
Interwire Cap	40	95	85	85	85	115

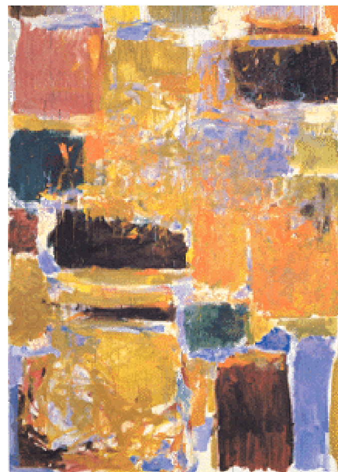
per unit wire length in aF/μm for minimally-spaced wires

Dealing with Capacitance

- To reduce parasitic wire capacitance, use low capacitance (low-k) dielectrics (insulators) such as polyimide or even air instead of SiO_2
  - family of materials that are low-k dielectrics must also be suitable thermally and mechanically and
  - compatible with (copper) interconnect
- Copper interconnect allows wires to be thinner without increasing their resistance, thereby decreasing interwire capacitance
- SOI (silicon on insulator) to reduce junction capacitance

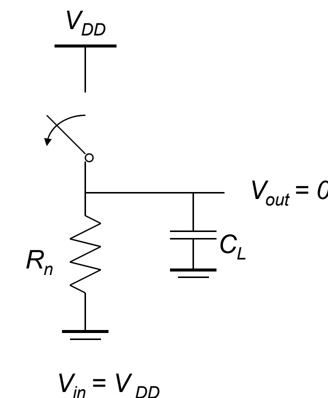
INTERCONNECT

Resistance

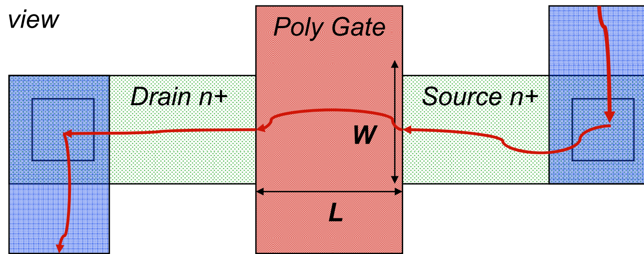


CMOS Inverter: Dynamic

- *Transient, or dynamic, response determines the maximum speed at which a device can be operated.*



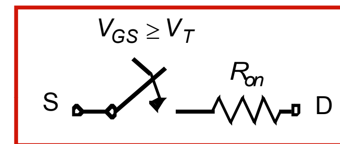
Sources of Resistance

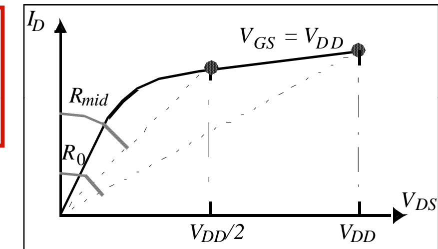


- MOS structure resistance - R_{on}
- Source and drain resistance – R_S, R_D
- Contact (via) resistance - R_C
- Wiring resistance - R_w

The Transistor as a Switch

- The simplest model assumes transistor as a switch with infinite “off” resistance, and a finite “on” resistance R_{on}.
- R_{on} is time varying, nonlinear and dependent on transistor operating point. Consider CMOS inverter: $V_{in}=0 \rightarrow V_{DD}$, $V_{out}=V_{DSn}=V_{DD} \rightarrow 0$. For propagation delay, we are interested in the time period from $t=t_1$ (when $V_{DSn}=V_{DD}$) to $t=t_2$ (when $V_{DS}=V_{DD}/2$), transistor works in saturation region and we use average value of resistances at the end points of the transition.

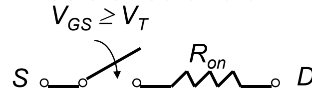




$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

MOS Structure Resistance

- The simplest model assumes the transistor is a switch with an infinite “off” resistance and a finite “on” resistance R_{on}

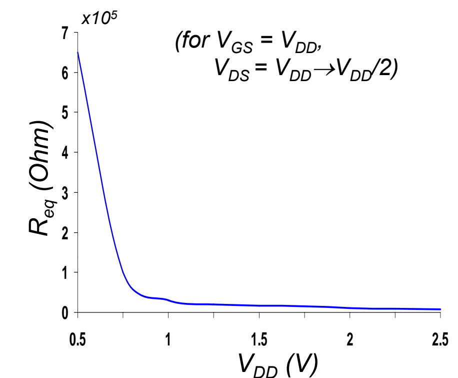


- However, R_{on} is nonlinear, so use instead the average value of the resistances, R_{eq}, at the end-points of the transition (V_{DD} and $V_{DD}/2$)

$$R_{eq} \approx ½ (R_{on}(t_1) + R_{on}(t_2))$$
$$R_{eq} = ¾ V_{DD}/I_{DSAT} (1 – 5/6 \lambda V_{DD})$$

Equivalent MOS Structure Resistance

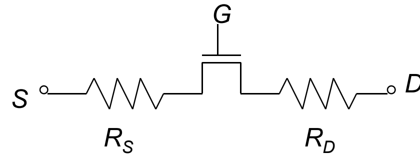
- The “on” resistance is inversely proportional to W/L. Doubling W halves R_{eq}
- For $V_{DD}>>V_T+V_{DSAT}/2$, R_{eq} is independent of V_{DD} (see plot). Only a minor improvement in R_{eq} occurs when V_{DD} is increased (due to channel length modulation)
- Once the supply voltage approaches V_T, R_{eq} increases dramatically



V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

R_{eq} (for W/L = 1), for larger devices divide R_{eq} by W/L

Source and Drain Resistance



$$R_{S,D} = (L_{S,D}/W)R_{\square}$$

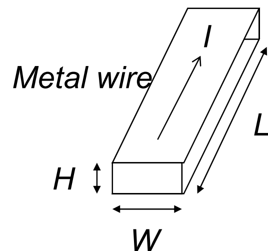
where $L_{S,D}$ is the length of the source or drain diffusion
$R_{\square}$ is the sheet resistance of the source or drain diffusion (20 to 100 $\Omega/\square$)

- More pronounced with scaling since junctions are shallower
- With silicidation $R_{\square}$ is reduced to the range 1 to 4 $\Omega/\square$
- Silicidation: cover drain/source regions with a low-resistivity material (e.g. Ti, W).

Contact Resistance

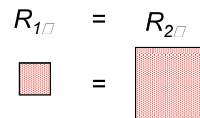
- Transitions between routing layers (contacts through via's) add extra resistance to a wire. To reduce contact resistance:
  - keep signals wires on a single layer whenever possible
  - avoid excess contacts
  - reduce contact resistance by making vias larger (beware of current crowding that puts a practical limit on the size of vias) or by using multiple minimum-size vias to make the contact
- Current crowding: Current tends to concentrate around the perimeter in a large contact hole.
- Typical contact resistances, R_C, (minimum-size)
  - 5 to 20 Ω for metal or poly to n+, p+ diffusion and metal to poly
  - 1 to 5 Ω for metal to metal contacts
- More pronounced with scaling since contact openings are smaller

Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho}{H}\frac{L}{W}$$

Sheet Resistance $R_{\square}$ (unit: $\Omega/\square$)



Resistance: $R = R_{\square} \cdot (L/W)$

Material	ρ(Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

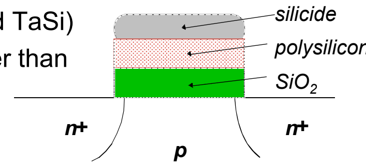
Sheet Resistance

- Al: low sheet resistance, preferred material for wiring of long interconnections.
- Poly-Si: large sheet resistance, only used for local interconnect.
- Use of diffusion wires should be avoided due to its large capacitance and associated RC delay.

Material	Sheet Resistance (Ω/□)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Overcoming Interconnect Resistance

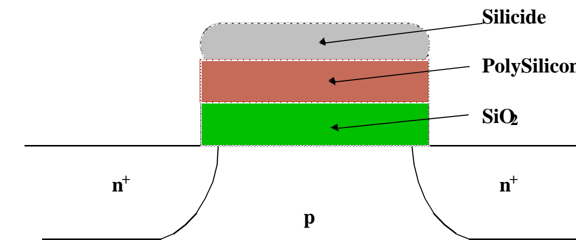
- Selective technology scaling:
  - scale W while holding H constant (If both W and H are scaled down, R_w would be too large)
- Use better interconnect materials
  - lower resistivity materials like copper
    - As processes shrink, wires get shorter (reducing C) but they get closer together (increasing C) and narrower (increasing R). So RC wire delay increases and capacitive coupling gets worse.
    - Copper has ~40% lower resistivity than aluminum, so copper wires can be thinner (reducing C) without increasing R
  - use silicides (WSi_2, $TiSi_2$, $PtSi_2$ and TaSi)
    - Conductivity is 8-10 times better than poly alone



- *Use more interconnect layers*
  - *reduces the average wire length L (but beware of extra contacts)*

Polycide Gate MOSFET

- Silicides: compound material formed using Si and a refractory metal. It's highly conductive and can withstand high-temperature process steps without melting.
- Polycide gate: combine poly-Si with upper coating of silicide. It has both good adherence and coverage (due to poly-Si) and high conductance (due to silicide).



Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly-Si

Example: Resistance of Metal Wire

- Ex: Calculate wire resistance if different materials (Al, Poly-Si, polycide) are used. Given: wire width W=1µm, wire length L=10cm. $R_□$ (Al)=0.075Ω/□, $R_□$ (poly-Si)=175Ω/□, $R_□$(polycide)=4Ω/□.
- Solution: If Al wire is used:

  $R_{wire}=\rho_□\times(L/W)=0.075\Omega/□\times(0.1m)/(1\times10^{-6}m)=7.5k\Omega$

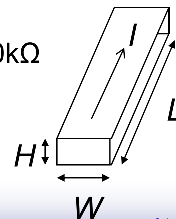
  If poly-Si is used for wire:

  $R_{wire}=\rho_□\times(L/W)=175\Omega/□\times(0.1m)/(1\times10^{-6}m)=17.5M\Omega$

  If polycide is used for wire:

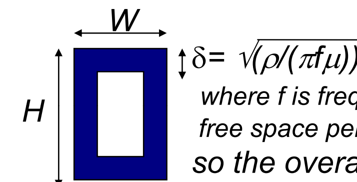
  $R_{wire}=\rho_□\times(L/W)=4\Omega/□\times(0.1m)/(1\times10^{-6}m)=400k\Omega$

  → Al is the best choice for wires!



Skin Effect

- Resistance also depends on frequency. At high frequency, currents tend to flow primarily on the surface of conductor with current density falling off exponentially with depth into the wire.
- Skin depth δ: depth at which current falls off to 1/e of its nominal value.



$\delta = \sqrt{\rho/(\pi f \mu)}$

δ= 2.6 µm for Al at 1 GHz

where f is frequency, ρ: resistivity of conductor, free space permeability: $\mu = 4\pi \times 10^{-7}$ H/m

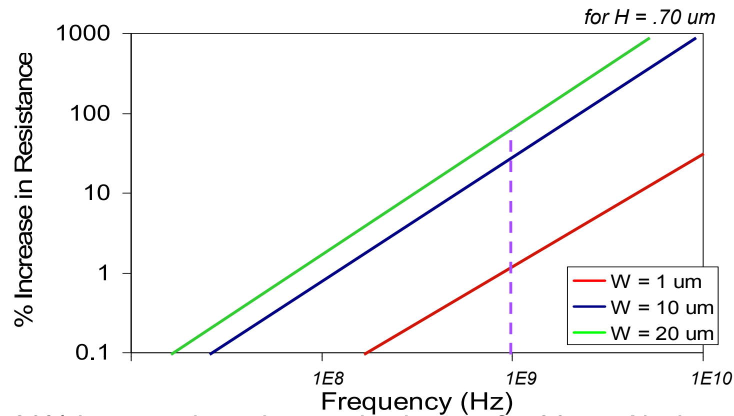
so the overall cross section is ~ 2(W+H)δ

- *Wire resistance per unit length at high frequency ($f>f_s$):* $r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H+W)}$
- *The onset of skin effect is at f_s - where the skin depth is equal to half the largest dimension (W or H) of the wire. For $f<f_s$, no skin effect. For $f>f_s$, skin effect must be considered.*

  $f_s = 4\rho / (\pi \mu (\max(W,H))^2)$

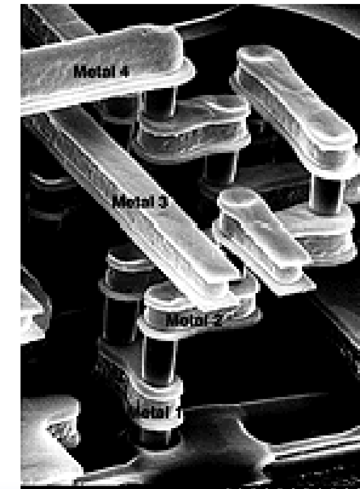
- *It's an issue for high frequency, wide(tall) wires (eg. clocks!)Why?*

Skin Effect for Different W's



- A 30% increase in resistance is observe for 20 μm Al wires at 1 GHz (versus only a 1% increase for 1 μm wires): skin effect is an issue for wider wires.
- Reason: for larger W, f_s is smaller, onset of skin effect is earlier. Note: $f_s = 4\ \rho / (\pi\ \mu\ (max(W,H))^2)$

Modern Interconnect

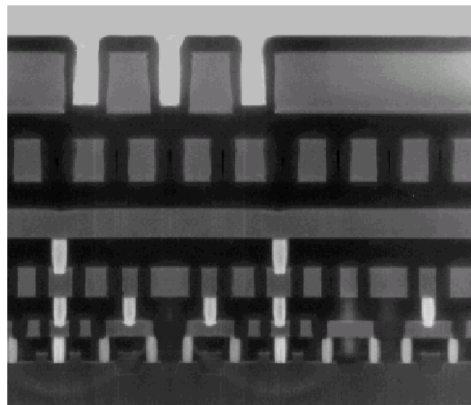


Example: Intel 0.25 micron Process

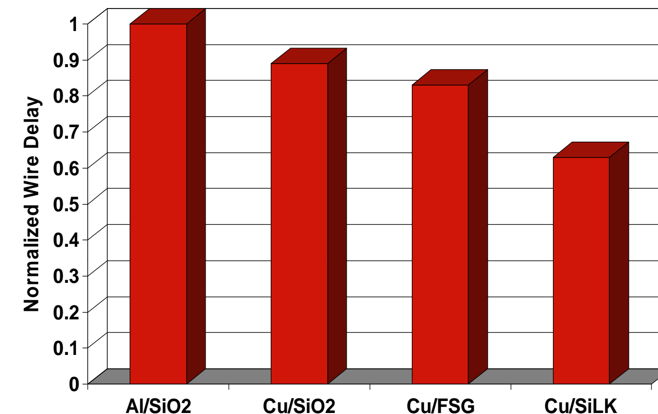
5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	μm	μm	

Layer pitch, thickness and aspect ratio



Comparison of Wire Delays



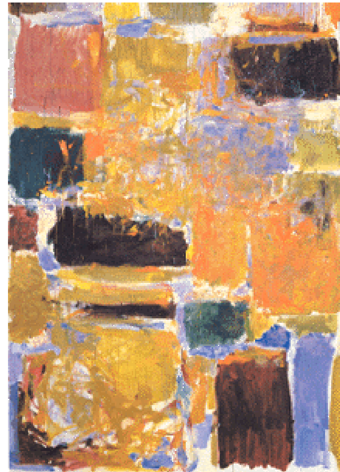
- FSG: flouro-silicate glass
- SiLK: a low-k (2.65) polymer material by Dow Chemical Company.

Compared to SiO_2, low k(dielectric constant) material reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation.

From MPR, 2000

INTERCONNECT

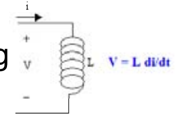
Inductance



Wire Inductance

- With adoption of low-resistive interconnect materials and increase of switching frequency to super-GHz range, inductance stats to play an important role.
- Inductance leads to inductive coupling between lines, and switching noise due to (Ldi/dt) voltage drops.
- Inductance: a changing current passing through an inductor generates a voltage drop: $\Delta V = L(di/dt)$
- Capacitance c and inductance l (per unit length) of a wire are related by equation: $cl = \varepsilon\mu$,

  ε, μ: permittivity and permeability of surrounding dielectric.



- Speed v at which an electromagnetic wave can propagate through the medium: $v = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$

  (c_0: speed of light in vacuum)

Example: Wire Inductance

- Ex: For Al1 wire on field oxide in 0.15µm CMOS technology, wire capacitance per unit length:

  c=(W×30+2×40) aF/µm,

  Find wire inductance per unit length (*l*) for wire widths of W=0.4µm, 1µm and 10µm. (Note: For SiO_2, $\varepsilon = 3.9 \times 8.85 \times 10^{-12}$ F/m, $\mu = 4\pi \times 10^{-7}$ H/m.)

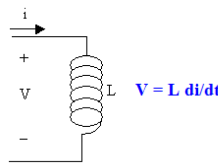
Solution: *cl=εµ, thus:*

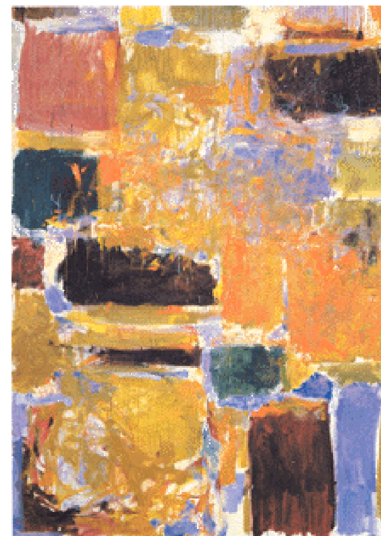
$l = \varepsilon\mu / c = (3.9 \times 8.85 \times 10^{-12}) \times (4\pi \times 10^{-7}) / c$

*For W=0.4*µm: c=92aF/µm; l=0.47pH/µm,

*For W=1*µm: c=110aF/µm; l=0.39pH/µm,

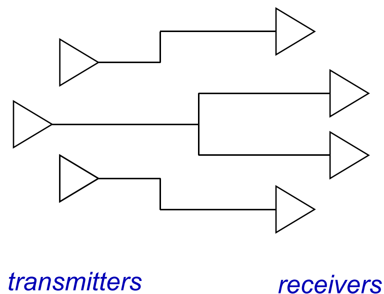
*For W=10*µm: c=380aF/µm; l=0.11pH/µm.

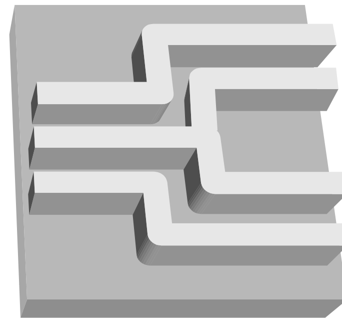




Interconnect Modeling

The Wire



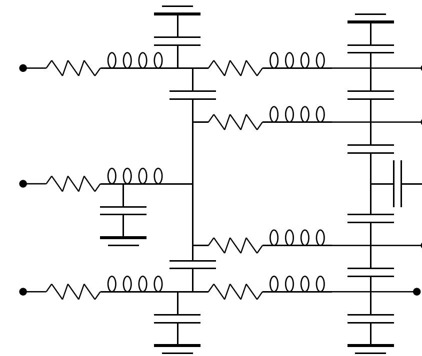


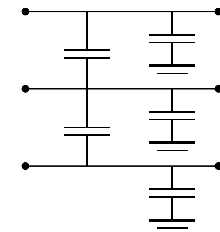
transmitters *receivers*

schematic *physical*

Wire Models

- *Interconnect parasitics (capacitance, resistance, and inductance)*
  - *reduce reliability*
  - *affect performance and power consumption*





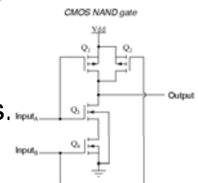
All-inclusive (C,R,I) model *Capacitance-only*

Parasitic Simplifications

- Inductive effects can be ignored
  - if the resistance of the wire is substantial enough (as is the case for long Al wires with small cross section)
  - if the rise and fall times of the applied signals are slow enough
- When the wire is short, or the cross-section is large, or the interconnect material has low resistivity, a capacitance only model can be used
- When the separation between neighboring wires is large, or when the wires run together for only a short distance, interwire capacitance can be ignored and all the parasitic capacitance can be modeled as capacitance to ground

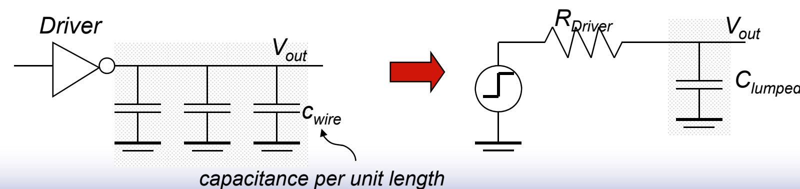
Wire Delay Models: Ideal Wire Model

- Ideal wire model
  - same voltage is present at every segment of the wire at every point in time – the whole wire is an equi-potential region.
  - A voltage change at one end of wire propagates immediately to its other ends, even if they are some distance away.
  - Eg. Wires in schematics: simple lines with no attached parameters or parasitics.
  - only holds for *very short* wires, i.e., interconnects between *very* nearest neighbor gates
  - Useful in early design phase when designer wants to concentrate on properties/behavior of transistors, or for small circuits with very short wires.



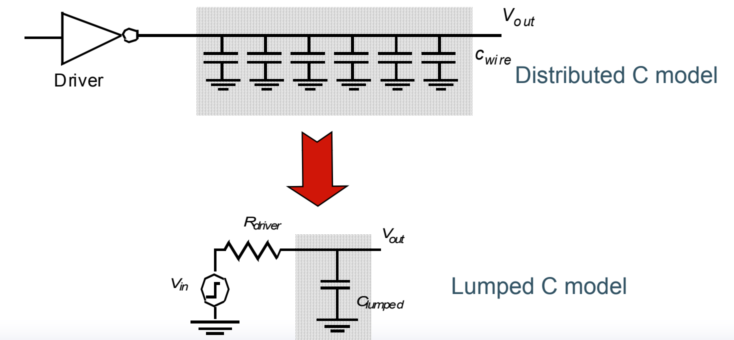
Wire Delay Models: Lumped C Model

- Lumped C model: good for short wires; pessimistic and inaccurate for long wires
  - when only a single parasitic component (C, R, or L) is dominant, the different fractions are lumped into a single circuit element
    - When the resistive component is small and the switching frequency is low to medium, can consider only C; the wire itself does not introduce any delay; the only impact on performance comes from wire capacitance



The Lumped C Model

- Lumped C model: $C_{lumped}=L\times c_{wire}$, where L: length of the wire, c_{wire}: wire capacitance per unit length.
- There are also lumped resistance model, lumped inductance model for wires.



Example: The Lumped C Model

- Assume driver with source resistance R_{driver}=10kΩ is used to drive a 10-cm-long, 1μm-wide Al1 wire. The total lumped capacitance of wire is 1pF. When applying a step input (V_{in}=0→V), find transient response of V_{out}, time to reach 50% point, and 10%-90% rising time of V_{out}.

Solution: $C_{lumped}(dV_{out}/dt)=(V_{in}-V_{out})/R_{driver}$.

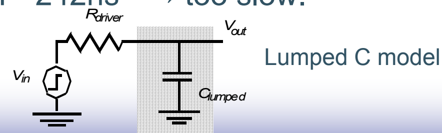
Thus: $V_{out}(t)=(1-e^{-t/\tau})V$, where time constant: $\tau=R_{driver}\times C_{lumped}$

Time for V_{out} to reach 50% point:

$t_{50\%}$=0.69×10kΩ×11pF=76ns → too slow.

Time for V_{out} to rise from 10%-90%:

$t_{90\%}$=2.2×10kΩ×11pF=242ns → too slow.

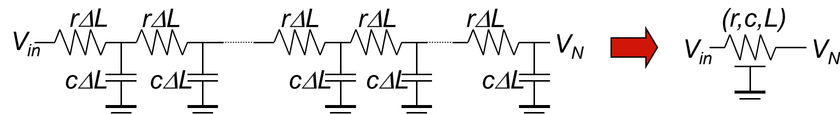


Wire Delay Models: Lumped RC Model

- Lumped RC model
  - For metal wires with L>1mm: resistance cannot be ignored. The equipotential assumption is no longer adequate. A resistive-capacitive model has to be adopted.
  - Lumped RC model: total wire resistance is lumped into a single R and total capacitance into a single C
  - good for short wires; pessimistic and inaccurate for long wires.
  - For long wires: distributed rc model should be used.

Wire Delay Models: Distributed RC Model

- Distributed RC model
  - circuit parasitics are distributed along the length, L, of the wire
    - c and r are the capacitance and resistance per unit length

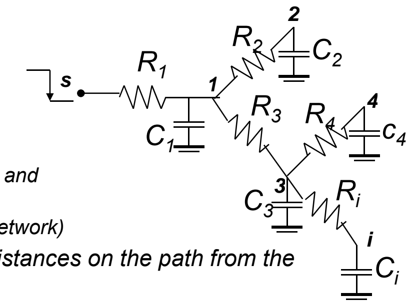


- *Delay is determined using the Elmore delay equation*

$$\tau_{Di} = \sum_{k=1}^{N} c_k r_{ik}$$

RC Tree Definitions

- *RC tree characteristics*
  - *A unique resistive path exists between the source node and any node of the network*
    - *Single input (source) node, s*
    - *All capacitors are between a node and GND*
    - *No resistive loops (i.e. it's a tree network)*



  - *Path resistance R_{ii}: sum of the resistances on the path from the input node to node i)*

$$R_{ii} = \sum_{j=1}^{i} R_j \Rightarrow (R_j \in [path(s \rightarrow i)]$$

Eg: Path resistance $R_{44}=R_1+R_3+R_4$

  - *Shared path resistance (resistance shared along the paths from the input node to nodes i and k)*

$$R_{ik} = \sum_{j=1}^{N} R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

Eg. Common path resistance: $R_{i4}=R_1+R_3$, $R_{i2}=R_1$.

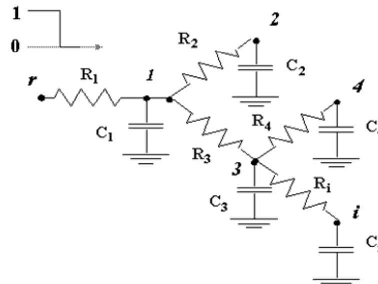
The Elmore Delay of RC Network

- Elmore delay: If step input is applied at source node s of a RC tree when t=0, Elmore delay from source node s to destination node i is:

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

where k: any node in network, N: total number of nodes in network.

- ✓ That is, Elmore delay from source node to destination node is the sum of each node capacitance multiplied by the shared path resistance from source node to this node and to the destination node.



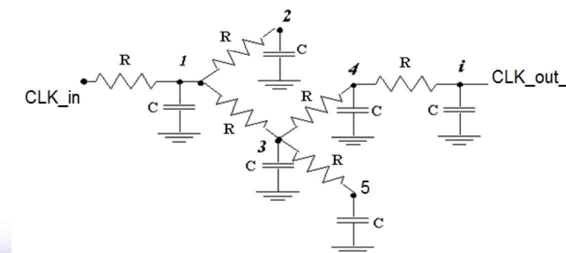
- Eg. Elmore delay for node i:

$$\tau_{Di} = R_1C_1+R_1C_2+(R_1+R_3)C_3+(R_1+R_3)C_4+(R_1+R_3+R_i)C_i$$

Example: The Elmore Delay

- Example: A clock distribution network is shown below. Calculate the Elmore delay t_d from clock driver (CLK_in) to a local clock (CLK_out_i), assume all the resistances are R, and all the capacitors are C.
- Solution: Elmore delay for t_d from clock driver (CLK_in) to a local clock (CLK_out_i):

$$\tau_{Di} = RC+RC+(R+R)C+(R+R+R)C+(R+R)C+(R+R+R+R)C = 13RC$$

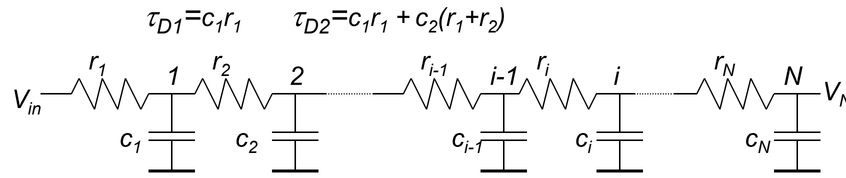


Chain Network Elmore Delay

- Simple nonbranched RC chain (or ladder):
  Elmore delay from V_{in} to V_N:

$$\tau_{DN} = \sum_{i=1}^{N} c_i r_{iN} = \sum_{i=1}^{N} c_i \sum_{j=1}^{i} r_j = \sum_{i=1}^{N} c_i r_{ii}$$

$\tau_{D1}=c_1r_1$ $\tau_{D2}=c_1r_1 + c_2(r_1+r_2)$



$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_i(r_1+r_2+\ldots+r_i)$

Assume $r_1=r_2=\ldots=r_N=r_{eq}$: $\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$

Elmore delay from V_{in} to V_N: $\tau_{DN}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_N(r_1+r_2+\ldots+r_N)$

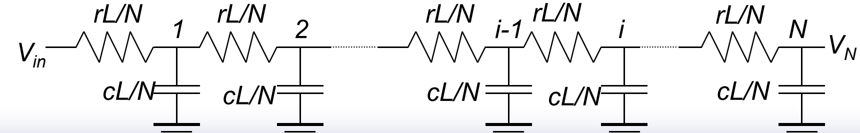
Distributed RC Model for Simple Wires

- A length L RC wire can be modeled by N segments of length L/N
  - The resistance and capacitance of each segment are given by r·L/N and c·L/N, Elmore delay of a distributed RC wire is:

$\tau_{DN} = (L/N)^2(cr+2cr+\ldots+Ncr) = (crL^2)\,(N(N+1))/(2N^2) = RC((N+1)/(2N))$

where r and c: resistance/capacitance per unit length; R (= rL) and C (= cL) are the total lumped resistance and capacitance of the wire,

- *For large N: Elmore delay:* $\tau_{DN} = RC/2 = rcL^2/2$
  - *Delay of a wire is a quadratic function of its length, L*
  - *The delay is 1/2 of that predicted by the lumped RC model. Using lumped RC model, delay is RC (pessimistic).*

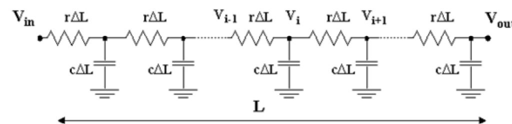


The Distributed RC-line

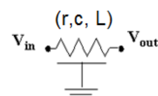
- Distributed RC line model: Diffusion equation

$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

Where: V: voltage at a particular point in the wire,
x: distance between this point and the signal source.



(a). distributed model



(b). Schematic symbol for distributed RC line

Step Response Points

Voltage Range	Lumped RC	Distributed RC
$0 \rightarrow 50\%$ (t_p)	0.69 RC	0.38 RC
$0 \rightarrow 63\%$ (τ)	RC	0.5 RC
$10\% \rightarrow 90\%$ (t_r)	2.2 RC	0.9 RC
$0 \rightarrow 90\%$	2.3 RC	1.0 RC

Time to reach the 50% point is t = ln(2)τ = 0.69τ

Time to reach the 90% point is t = ln(9)τ = 2.2τ

- Example: Consider a Al1 wire 10 cm long and 1 μm wide
  - Using a lumped C only model with a source resistance (R_{Driver}) of 10 kΩ and a total lumped capacitance (C_{lumped}) of 11 pF

    $t_{50\%}$ = 0.69 x 10 kΩ x 11pF = 76 ns

    $t_{90\%}$ = 2.2 x 10 kΩ x 11pF = 242 ns
  - Using a distributed RC model with c = 110 aF/μm and r = 0.075 Ω/μm

    $t_{50\%}$ = 0.38 x (0.075 Ω/μm) x (110 aF/μm) x (10^5 μm)^2 = 31.4 ns

    $t_{90\%}$ = 0.9 x (0.075 Ω/μm) x (110 aF/μm) x (10^5 μm)^2 = 74.25 ns

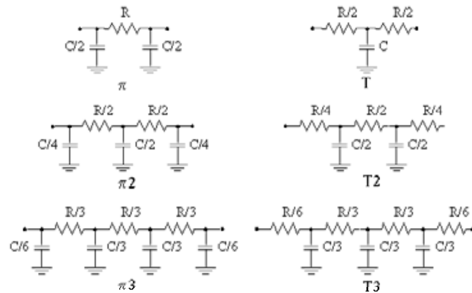
Poly: $t_{50\%}$ = 0.38 x (150 Ω/μm) x (88+2×54 aF/μm) x (10^5 μm)^2 = 112 μs

Al5: $t_{50\%}$ = 0.38 x (0.0375 Ω/μm) x (5.2+2×12 aF/μm) x (10^5 μm)^2 = 4.2 ns

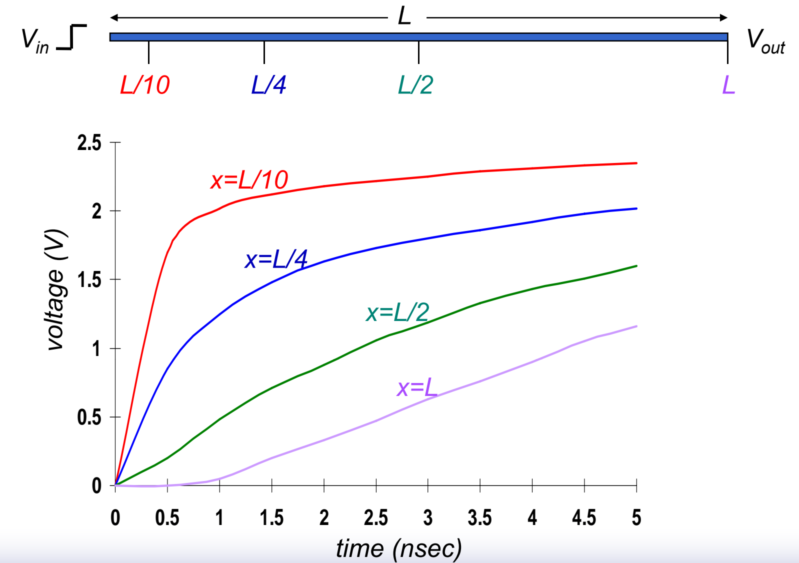
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Simulated Step-response of RC Wire



Design Rules of Thumb

- rc delays should be considered when $t_{pRC} > t_{pgate}$ of the driving gate

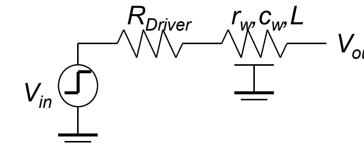
$$L_{crit} > \sqrt{t_{pgate}/0.38rc}$$

  - actual L_{crit} depends upon the size of the driving gate and the interconnect material
- rc delays should be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

  - when not met, the change in the signal is slower than the propagation delay of the wire so a lumped C model suffices

Putting It All Together



- *Total propagation delay consider driver and wire*

$$\tau_D = R_{Driver}C_w + (R_wC_w)/2 = R_{Driver}C_w + 0.5r_wc_wL^2$$

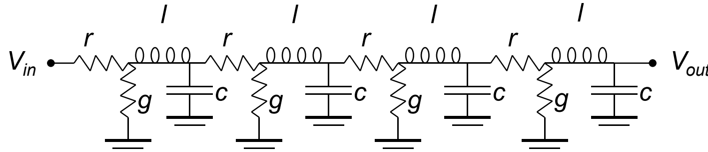
and $t_p = 0.69\, R_{Driver}C_w + 0.38\, R_wC_w$

where $R_w = r_wL$ *and* $C_w = c_wL$

- *The delay introduced by wire resistance becomes dominant when* $(R_wC_w)/2 \geq R_{Driver}\, C_W$ *(when* $L \geq 2R_{Driver}/R_w$*)*
  - *For an* R_{Driver} *= 1 kΩ driving an 1 μm wide Al1 wire,* L_{crit} *is 2.67 cm*

Inductance

- When the rise and fall times of the signal become comparable to the time of flight of the signal waveform across the line, then the inductance of the wire starts to dominate the delay behavior



- Must consider wire transmission line effects
  - Signal propagates over the wire as a wave (rather than diffusing as in rc only models)
    - Signal propagates by alternately transferring energy from capacitive to inductive modes

More Design Rules of Thumb

- Transmission line effects should be considered when the rise or fall time of the input signal (t_r, t_f) is smaller than the time-of-flight of the transmission line (t_{flight})

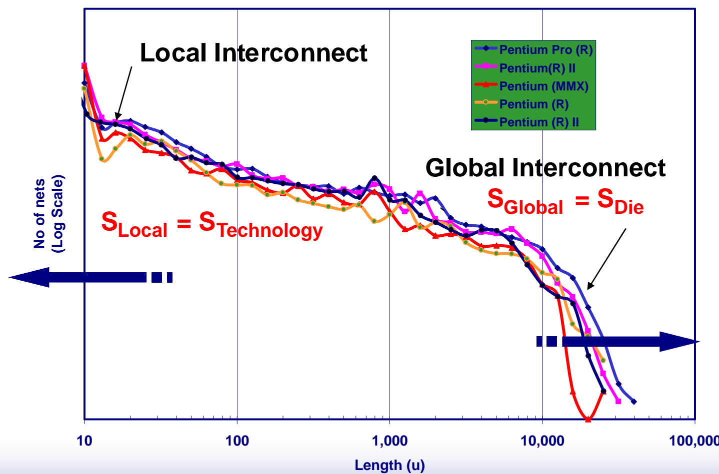
$$t_r \ (t_f) < 2.5\ t_{flight} = 2.5\ L/v$$

  - For on-chip wires with a maximum length of 1 cm, we only worry about transmission line effects when $t_r <$ 150 ps

- Transmission line effects should only be considered when the total resistance of the wire is limited

$$R < 5\ Z_0 = 5\ (V/I)$$

Nature of Interconnect



Wire Spacing Comparisons