

بسم الله الرحمن الرحيم

Republic of Iraq
The Ministry Of Higher Education
& Scientific Research



University: Diyala
College: Engineering
Department: Computer
Stage: Second
Lecturer name: Roadia Abdullah
Qualification: Master
Place of work: Computer Dept.

Course Instructor	Roadia Abdullah				
E-mail					
Title	Computer Architecture				
Course Coordinator	Roadia Abdullah				
Course Objective	تعريف الطالب على المكونات الحاسبة و كيف تتعامل فيما بينها و المعمارية التي تم على اساسها بناء الحاسبة و تعرف على كل الجوانب المهمة في معمارية و عمل الحاسبة				
Course Description	١. Basics of Computer System. ٢. Computer System Design (Basic Computer Design). ٣. Microprogramming Control. ٤. Memory Organization. ٥. I/O Organization. ٦. Optional Topics.				
Textbook	Computer System Architectures M. Mano				
Course Assessments	Term Tests	Laboratory	Quizzes	Project	Final Exam
	As(٣٠%)	As(١٠%)	As(١٠%)	-	As(٦٠%)
General Notes					

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Course Weekly Outline

Week	Date	Topics Covered	Lab. Experiment Assignments	Notes
١	٢٣/٠٩/٢٠١٤	١.١ Introduction and review of logic concepts ١.٢ Block diagram of computer system		
٢	٣٠/٠٩/٢٠١٤	١.٣ Buses ١.٤ Fetch –execute cycle		
٣	٠٧/١٠/٢٠١٤	١.٥ Classifications of machines ١.٦ Computer instruction set and its classification		
٤	١٤/١٠/٢٠١٤	١.٧ Addressing modes. ١.٨ Stack organization. ١.١٠ RISC CISC and overlapped register windows		
٥	٢١/١٠/٢٠١٤	٢.١ Basic computer organization ٢.٢ Basic computer Instruction format and stored program organization		
٦	٢٨/١٠/٢٠١٤	٢.٣ Basic computer addressing modes and instruction types.		
٧	٠٤/١١/٢٠١٤	٢.٤ Basic computer timing and control		
٨	١١/١١/٢٠١٤	٢.٥ Register transfer and micro operations		
٩	١٨/١١/٢٠١٤	٢.٦ Design of basic computer Arithmetic Logic Unit (ALU).		
١٠	٢٥/١١/٢٠١٤	٢.٧ Design of basic computer hardware control unit.		
١١	٠٢/١٢/٢٠١٤	٢.٨ Bus and memory transfer ٢.٩ Input-Output and Interrupt of basic computer		
١٢	٠٩/١٢/٢٠١٤	٢.١٠ Programming of basic computer		
١٣	١٦/١٢/٢٠١٤	٢.١١ Complete description of basic computer.		
١٤	٢٣/١٢/٢٠١٤	٢.١٢ Machine characteristics and performance		
١٥	٣٠/١٢/٢٠١٤	٣.١ Control memory ٣.٢ Address sequencing		

١٦	٠٦/٠١/٢٠١٥	End Term Exam		
١٧	١٧/٠٢/٢٠١٥	٣.٣ Design of control unit ٣.٤ Micro program sequencer ٣.٥ Example on the control unit		
١٨	٢٤/٠٢/٢٠١٥	٤.١ Memory hierarchy ٤.٢ Main memory		
١٩	٠٣/٠٣/٢٠١٥	٤.٣ Auxiliary memory ٤.٤ Associative memory		
٢٠	١٠/٠٣/٢٠١٥	٤.٥ Cache memory ٤.٦ Virtual memory		
٢١	١٧/٠٣/٢٠١٥	٤.٧ Page replacement		
٢٢	٢٤/٠٣/٢٠١٥	٤.٨ Memory management hardware		
٢٣	٣١/٠٣/٢٠١٥	٤.٩ Memory protection		
٢٤	٠٧/٠٤/٢٠١٥	٥.١ Peripheral devices and ASCII code ٥.٢ I/O Interface		
٢٥	١٤/٠٤/٢٠١٥	٥.٣ I/O versus memory bus ٥.٤ Isolated versus memory-mapped I/O		
٢٦	٢١/٠٤/٢٠١٥	٥.٥ Asynchronous data transfer ٥.٦ Parallel priority interrupt		
٢٧	٢٨/٠٤/٢٠١٥	٥.٧ FIFO buffer ٥.٨ Modes of transfer		
٢٨	٠٥/٠٥/٢٠١٥	٥.٩ Direct Memory Access (DMA) ٥.١٠ I/O processor		
٢٩	١٢/٠٥/٢٠١٥	٥.١١ Serial communication ٥.١٢ Examples on the I/O devices		
٣٠	١٩/٠٥/٢٠١٥	٦.١ Arithmetic algorithms		
٣١	٢٦/٠٥/٢٠١٥	٦.٢ Pipeline processing		
٣٢	٠٢/٠٦/٢٠١٥	End Term Exam		

INSTRUCTOR Signature:

Dean Signature: