Ministry Of Higher Education

And Scientific Research

University Of Diyala

College Of Engineering

CommunicationEngineering Department

Design And Implementation Of Digital Frequency Meter

A project

Submitted to the Department of Communication University of Diyala-College of Engineering in Partial Fulfillment of the Requirement for Degree Bachelor in Communication Engineering

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بسم الله الرحمن الرحيم

(وَقُلِ اعْمَلُوا فَسَيَرَى اللَّهُ عَمَلَكُمْ وَرَسُولُهُ وَالْمُؤْمِنُونَ)

صدق الله العظيم

سورة التوبة *105*

Dedication

TO

MY " FAMILY " WITH LOVE

Acknowledgement

understanding and support We wish to thank our family for their including our parents, siblings , our big family and our friends inside and outside university.

We wish to express our deepest gratitude to our Advisors Msc. Abud Al-monam Ahmed and Msc. OmarAbud Al-kareem for our guidance and friendship during our study. And at last we want to thank the department of communication for giving us the chance to work on as a fine project as this one.

وزارة التعليم العالي والبحث العلمي

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ABSTRACT

The digital frequency meters are widely used in generating stations to measure the frequency of any incoming signals to the system. This device is useful for monitoring the frequency and auto controlling its by adjustment of prim-mover and other applications. In this project an introduction about the digital frequency meter was introduced and the application of this device in generating stations. The design of digital frequency meter is implemented and carried out experimentally by using integrated circuits (ICs). The family of (CMOS) was used in this design. Finally, the results that obtained by the new design of digital frequency meter shows that the new device of digital frequency meter is comfortable for measuring the frequency of signals within specific range of frequencies (1-999 Hz) in generating stations and other applications.

الملخص

مقياس التردد الرقمي يستخدم بكثره في محطات التوليد لاغراض المراقبة والسيطره على المنظومه والتطبيقات الاخرى، في هذا البحث قد تم توضيح الفكره الرئيسيه لعمل مقياس التردد الرقمي وتطبيقاته، وتم تصميم وبناء هذا الجهاز عمليا بأستخدام الدوائر المتكامله وقد استخدم نوع (CMOS) لهذا التصميم، اخيرا قد بينت النتائج التي تم الحصول عليها من عمل هذا الجهاز انه مناسب لقياس تردد اي اشاره في المنظومه ضمن مدى ترددي(1-999 HZ) في محطات التوليد والتطبيقات اخرى.

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LED	-	light Emitting Diode
LCD	-	Liquid Crystal Display
BCD	-	Binary Code Decimal
LE	-	Latch Enable
ZCD	-	Zero Crossing Detector

LIST OF SYMBOLS

I_L Load current.

V_L Load voltage.

F The frequency of the voltage Waveor current wave.

R_t The total equivalent resistance of the load.

C The total capacitance of the load.

LThe total inductance of the load.

NsThe speed of the rotor of the generatorin (r.p.m).

PThe number of poles of generator.

G_1,G_2 Displacement

I_1,I_2Currents

T1,T2 Torques

I_cCapacitor current

I_R Resistance current

V_mThe maximum value of supply voltage

$\tau 2, \tau 1$Time

C1,C2 Capacitance

F_{osci}The scan oscillator frequency of multiplexer

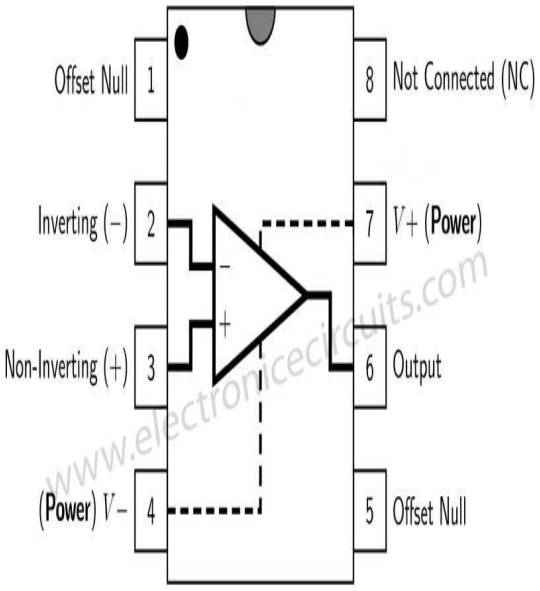
Chapter Three

Hardware Implementation of Digital Frequency Meter

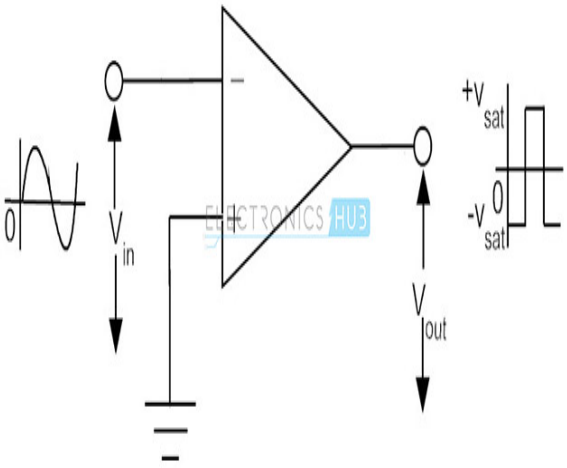
In this chapter, we will discuss and implementation each diagram by using integral circuit(ICS).**[4]**

3.1 Implementation of the Zero-Crossing Detector (ZCD)

In last few chapters we said that the zero crossing detector can done by using a comparator, this comparator is represented by an ordinary operation amplifier (op-amp), there are several types of the op – amps that were manufactured by many companies of electronics, the more commonly used is (741 IC), Fig. (3.1) shows this op-amp, Fig.(3.1a) shows the out pins connection, and Fig.(3.1b) shows the block diagram of the connection to use 741 as a (ZCD) to convert the sine wave to a square wave.



(a)Top view pin connection of (741IC)as (ZCD)



(b) The block diagram to connect (741 IC) as (ZCD)

Fig.(3.1) : Connection (741IC) as (ZCD)

To analyze the operation of the circuit in Fig.(3.1b), we assume a sine wave input to the op – amp circuit, the input voltage is connected to pin (3) that represents the non – inverting input, while pin (2), which is the inverting input of the op – amp is connected to the ground to ensure that the input voltage is compared with ground (zero voltage), whenever the input voltage is positive the output of the op – amp is high (logic 1) while when it less than zero (negative) the output is low (logic 0) than Fig.(3.2) shows the input and output wave forms.

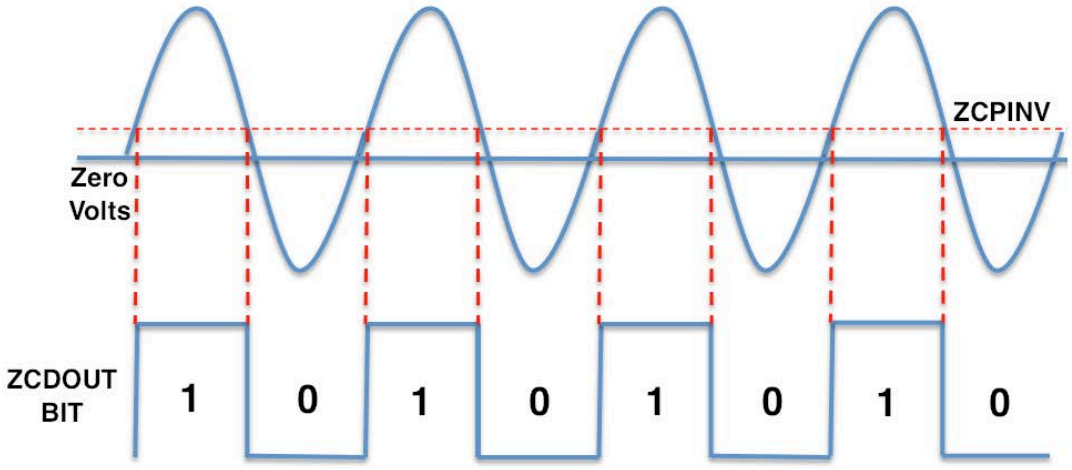


Fig.(3.2) : The input and output of wave forms of the (ZCD)

In Fig.(3.2) that represents the whole circuit connection of the digital frequency meter, we can see that the (ZCD) input is connected to a potentiometer output to control the value of maximum voltage sine wave input that makes the instrument measure, the frequency of high voltage signal without the need to attenuate them by any external attenuator because the potentiometer attenuates them to a suitable voltage, for example, if we want to measure the frequency of (250 v AC) sine wave while our circuit work with (5 v DC) and the (ZCD) can accept at most (±15 V peak),then if we use the potentiometer with the ration

$\frac{5*\sqrt{2}}{220} \cong \frac{1}{62}$then the maximum input voltage = $250_{rms}*\sqrt{2}$ =±353.3v_{peak}

Vout peak = $\pm 353.3*\frac{1}{6} = \pm 5.7 V_{peak}$

As shown in Fig.(3.3)

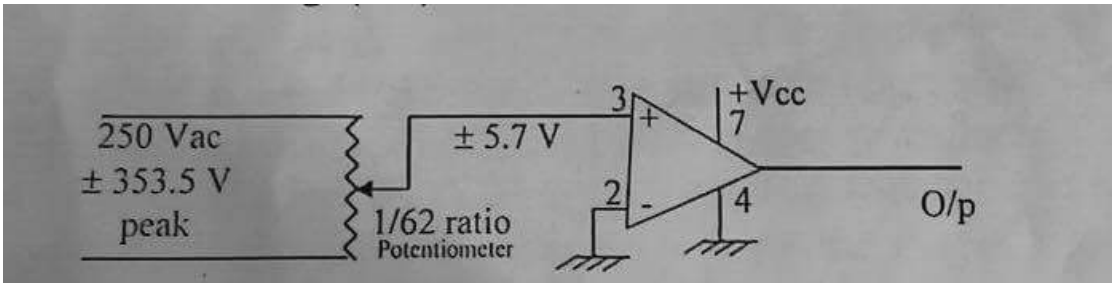


Fig.(3.3) : The use of the potentiometer with op-amp

3.2 Implementation of counter gate:

A counter gate as mentioned in chapter two was a simple (AND) gate or (NAND) gate.

In our case we use a two input (NAND) gate, this (NAND) gate is found in integral circuit of number (4011 CMOS), Fig.(3.4) shown below explain the block diagram and output pins connection of (4011) IC.

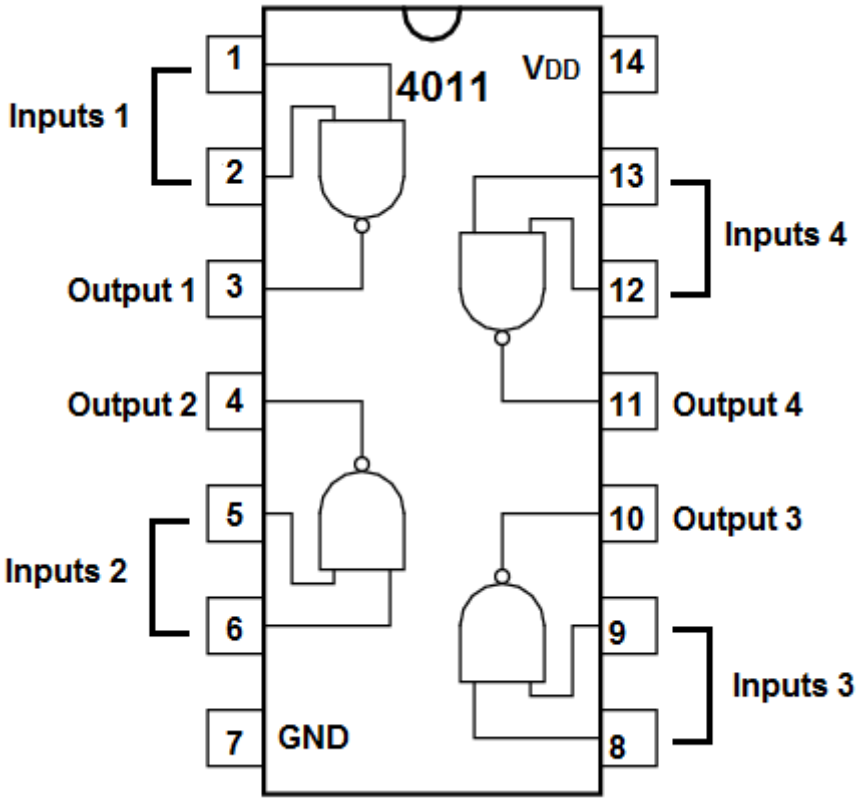


Fig.(3.4) : Block diagram of 2 –input (NAND)gate

3.3 Implementation Of Timing and Control Signal Generating Block:

As before mentioned in chapter two, there are types of pulses, the first is the signal of exact one second goes to counter gate, the width of this pulse is very important in the accuracy of digital frequency meter, in practical circuit we generate this signal from crystal oscillator with high frequency and suitable divider, the oscillator and the 14 stage binary divider and Dual JK-FF (neg Edge trig) are found in the integrate circuit of number (4060) and (74107), the (4060) IC and (74107)IC will be discussed in this section.

The second and third types of signals are the latch enable signal and reset counter pulse, the width of this signal can be designed as we like but the position of them in relation to each other and to first type signal is very important and if you return to fig.(2.4), we can see the shape and position of each signal.

Latch shape signal and reset counter signal are generating from two monostablemultivibrators which are found in the integrated circuit of number (4538) IC. Now we discuss the connection of (4060 and 4538 ICs).

3.3.1 The connection of (4060) Integrated Circuit

A 14- Stage ripple carry binary counter with oscillator are found in a dual – in – line (DIP) package of number (4060) is shown in Fig (3.5)below:

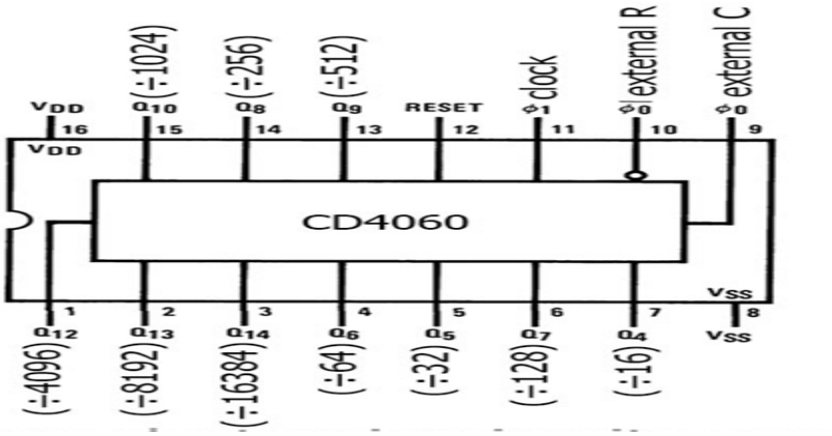


Fig.(3.5) : Connection diagram of (4060) IC

3.3.2 Implementation of frequency divider by using (74107) IC

As we said before the divider is used to divide by (N),to implement this divider we use CMOS (74107) IC as a divided by (4) divider. Fig.(3.6) shows the top view of (74107) IC and output pins connection.

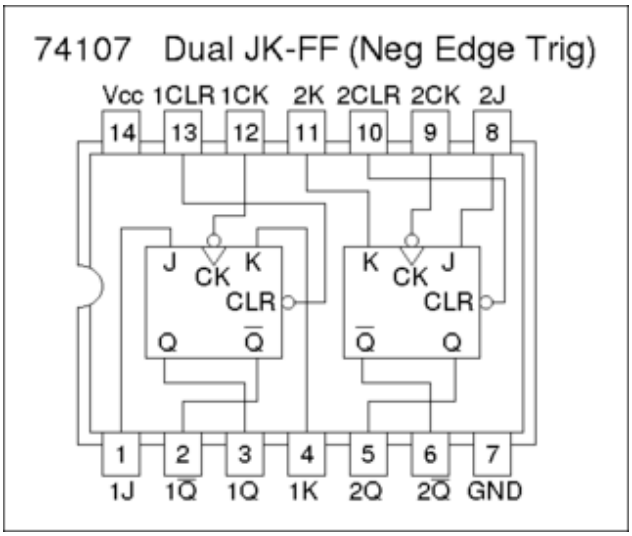


Fig.(3.6) : Out put pin connection of (74107)

3.3.3 The Connection of (4538) IC

The dual precision monostablemultivibrator is an integrated circuit contains from two monostablemultivibrators. These two monostablesmultibibrators are used to generate the latch enable signal and reset counters signal, these two signal position are alternate to each other, the latch enable (LE) generate with (τ1) width then the reset counter signal (RESET) generate with width (τ2), the sehematicdiagrame and connection of (4538 C-MOS) IC is shown in fig.(3.7) below.

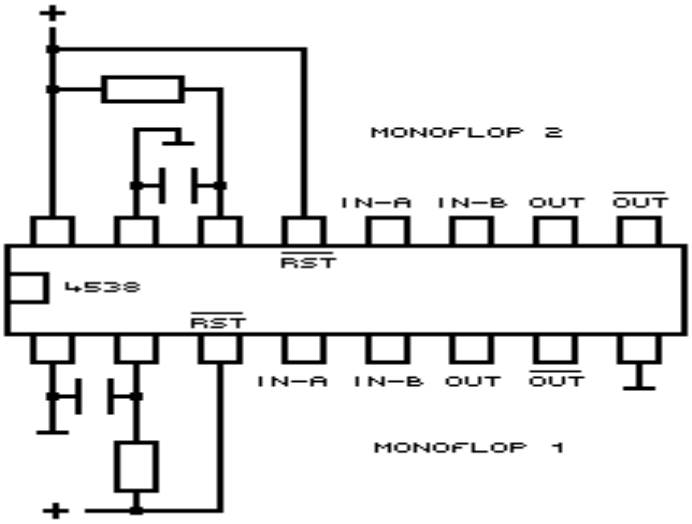


Fig.(3.7) : Block diagram of (4538)IC

To design ($\tau 1$ and $\tau 2$) with suitable time we can calculate the value of (R1, R2, C1 and C2) from the following equation:

$\tau 1 = \ln 2 \,.\, R1.\, C1$

$\tau 2 = \ln 2 \,.\, R1.\, C2$ ……(3.1)

In our case we chose ($\tau 1 = 1\ \mathrm{m}\,.\,\mathrm{sec}$ and $\tau 2 = 1\ \mathrm{m}\,.\,\mathrm{sec}$) also, then from equation (3.1) we can calculate (R1, R2, C1, and C2) as follows:

Let C1= C2 =100 nF, $\tau 1 = \tau 2 = 1 * 10^{-3}$ sec

Then R1=R2 = 14.426 KΩ

3.4 Implementation of the BCD Counters and the latch (4553) IC

As we said before we use three digits (BCD) counters to count from (000 –to -999) pulses, the three (BCD) counter each of four-bits can be obtained by using (4553 COMS) IC, that consist of three negative edge-triggered (BCD) counters which are cascaded in a synchronous fashion, A quad latch at the output of each of the three BCD counters permits storage of any given count, the three sets of BCD outputs (active high), after going through the latches, are timing division multiplexed, providing one BCD number or digit at a time .Digit select output(active low or LE) signal are provided for display control that as we said be for controlled by (LE) signal that came from controlling block.

This (4553 CMOS) IC consists also a built-in oscillator to multiplex the BCD output numbers with required frequency that must be not less than (60 or 50HZ) for each number, this An on-chip oscillator provides the low frequency scanning clock which drives the Multiplexer output selector, the frequency of the oscillator can be controlled externally by capacitor between pin 3 and pin 4 as shown in fig (3.8), multiple devices can be cascaded using overflow output with provides one pulse for every 1000 counts.

Referring to fig (3.8), the (Master Reset) input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit, while (Master Reset) is high the digital scanner is set to digit one, but all three digit select output are disabled to prolong display life, and the scan oscillator is inhibited.

The Disable input (pin11), where high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times, information present in the counter when the latch input goes high, will be stored in the latches and will be retained while the latch is high, independent of other inputs, information can be recovered from the latches after the counters have been reset, if (Latch Enable LE) remains high during entire rest cycle

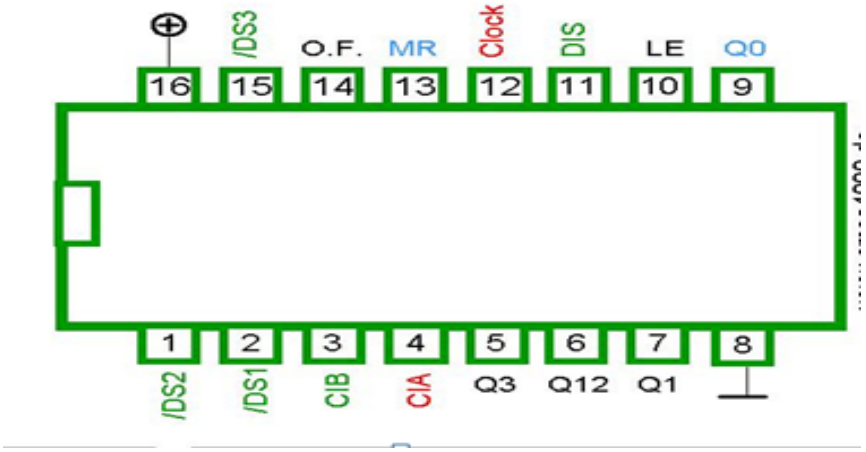


Fig.(3.8) : Block diagram of (4553 C-MOS) IC

To find the value of (C_1) which determines the frequency of output multiplexing frequency, data sheet of (4553 C – MOS) IC gives the following equation:

$f_{OSCi} = \frac{0.4\ Hz}{C1\ \mu F}$ at Vcc – GND= 5V …… (3.2)

Where:

$f_{osci.}$- The scan oscillator frequency of multiplexer.

Then the frequency of each digit equal($\frac{fosci}{3}$), if we choose the frequency of each digit equal to (1 KHz), the f_{osci} =3 * 1 KHz = 3 KHz

C1 = $\frac{0.4}{3}$ KHz = 0.1333 µF

3.5 Implementation of the BCD to Seven – Segment Decoder and Driver

We use BCD to seven – segment decoder, since we use a multiplexer with the output of three _ digits counter we use one decoder only instead of three decoder because of the use of multiplexer.

A BCD - to – seven segment latch decoder / driver for (LED) or liquid crystals display is a (4543 CMOS) IC, this circuit provides the function of a 4 – bits storage latch and an (8421) BCD to seven segment decoder and driver, the device has the

capability to inverse the logic levels of the output combination, the phase (PH), blanking (BI), and latch display (LD) inputs are used to reverse the truth table phase, blank the display and stored BCD code.

The phase (ph) is in a low state because we use a common cathode (LED) display and (ph) is high if we use common anode (LED) display.

Fig. (3.9) shows the output pins connection of (4543 CMOS) IC.

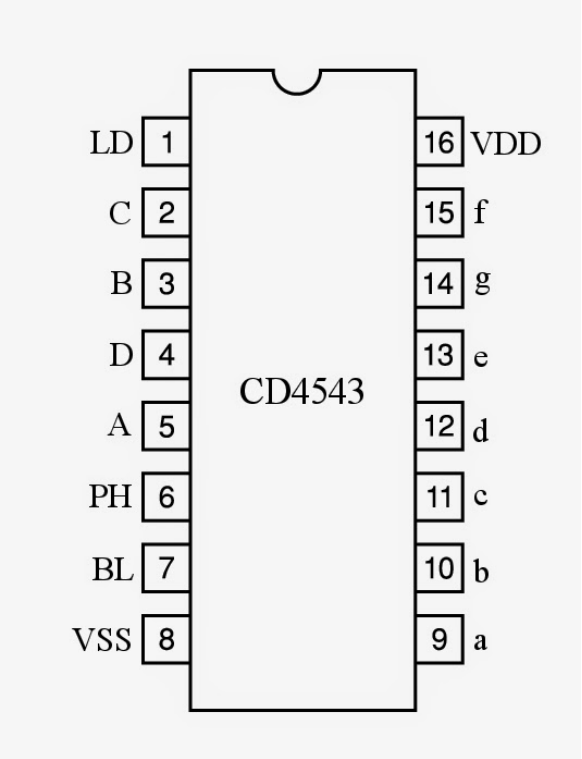


Fig.(3.9) : The out put pins connection of (4543 C-MOS)IC

For more information about the (4543 C – MOS) IC working we can see Fig.(3.10) that represent internal block diagram of this IC.

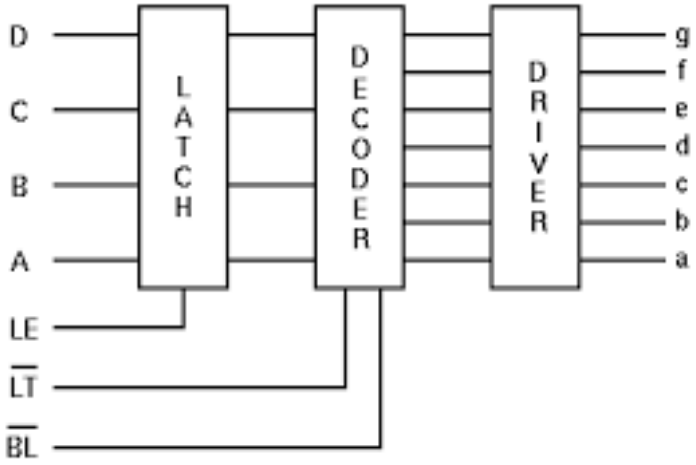


Fig.(3.10) : Block diagram of (4543 CMOS) IC

3.6 The implementation of three – digit light emitting diode (LED) display

From more simplicity in output connection to the (LED) display we use common cathode 3- digits input multiplexed (LED) seven – segment display, the internal connection of this display is as shown in Fig.(3.11). We use 3- PNP transistor and seven resistance with this LED display to control the bits current and the multiplexing of each digit of them as shown in Fig.(3.11) that presents the whole connection of accuratedigital frequency meter circuit.

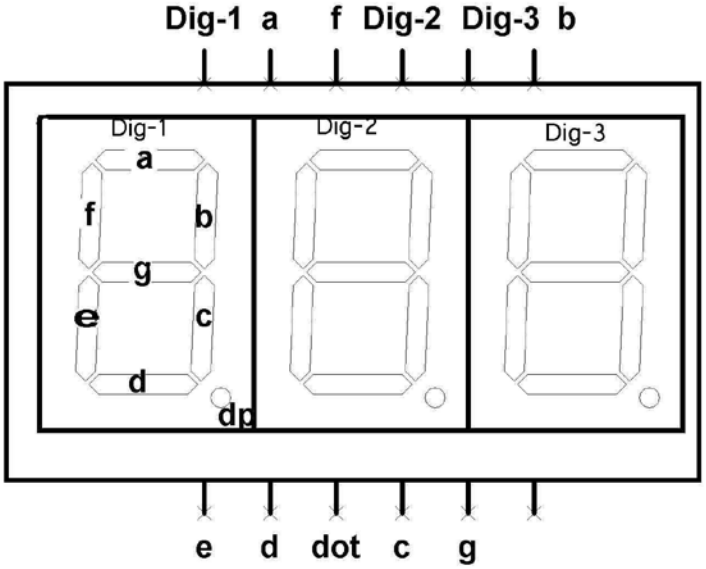


Fig.(3.11) : The internal connection of this display

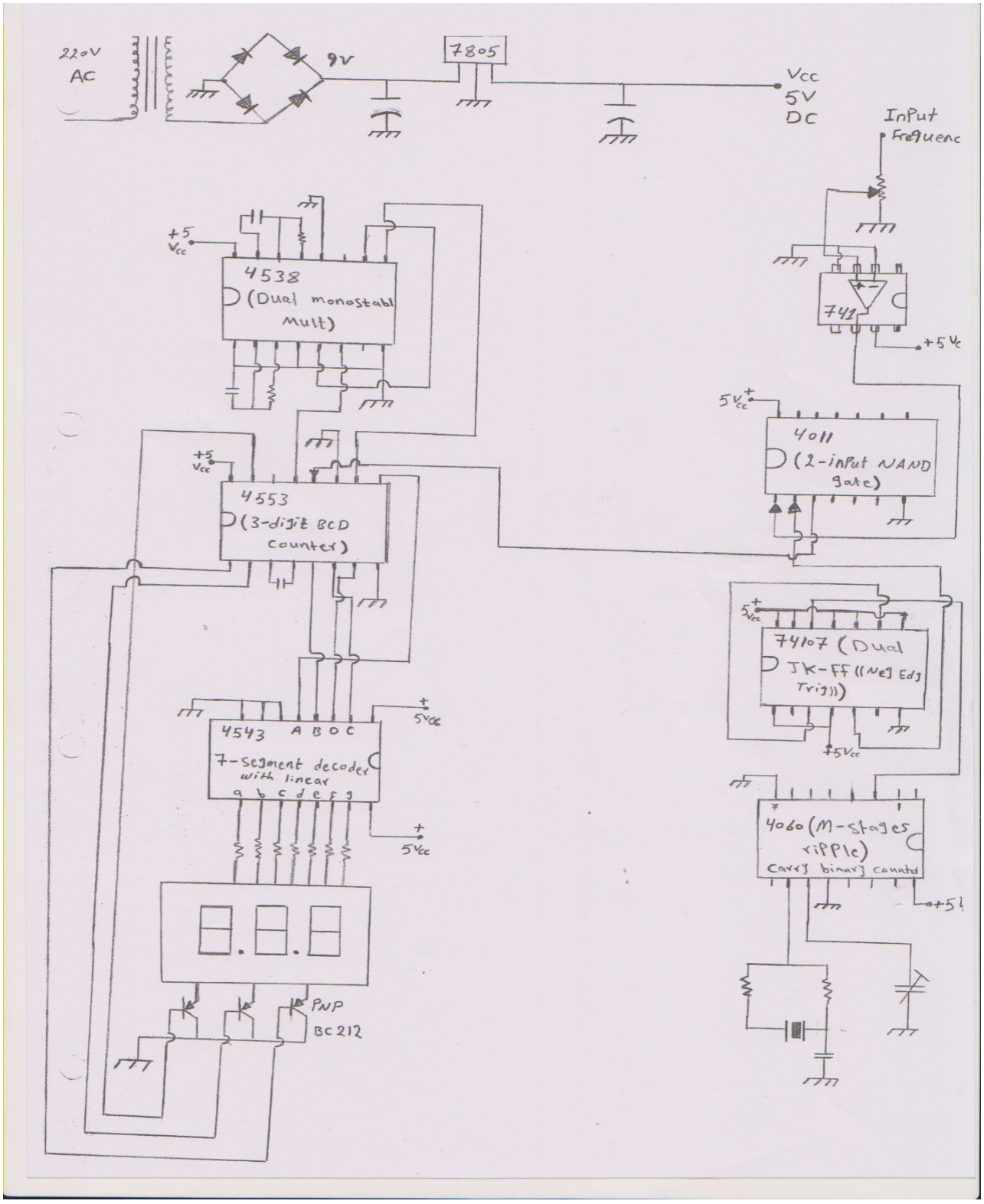


Fig.(3.12) Circuit diagram and connection of digital frequency meter

Chapter four

Result ,conclusion and future works

4.1 Testing of digital frequency meter

In the last two chapter, We were able to design a digital device consists of a number of electronic components to measure the incoming signal frequency to any source within a specific range of frequencies from a (1 Hz -999 Hz).

We can see the stages of each part of the electronic components that growth device which is designed in the following formats in this chapter.

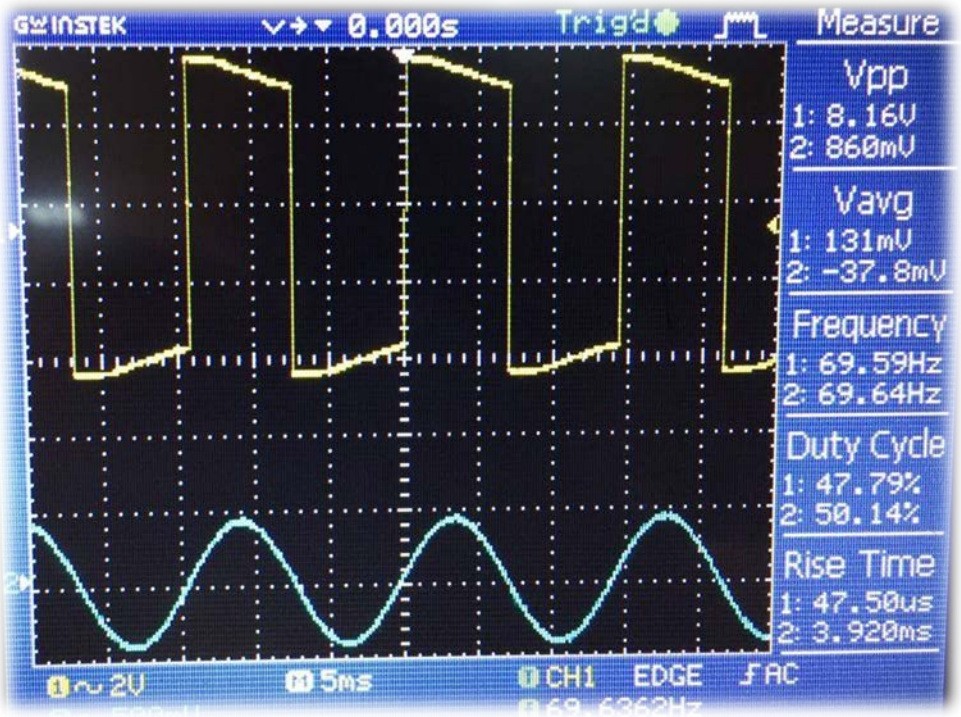


Fig.(4.1) : Reading of input sine wave and out put zero crossing amplifier

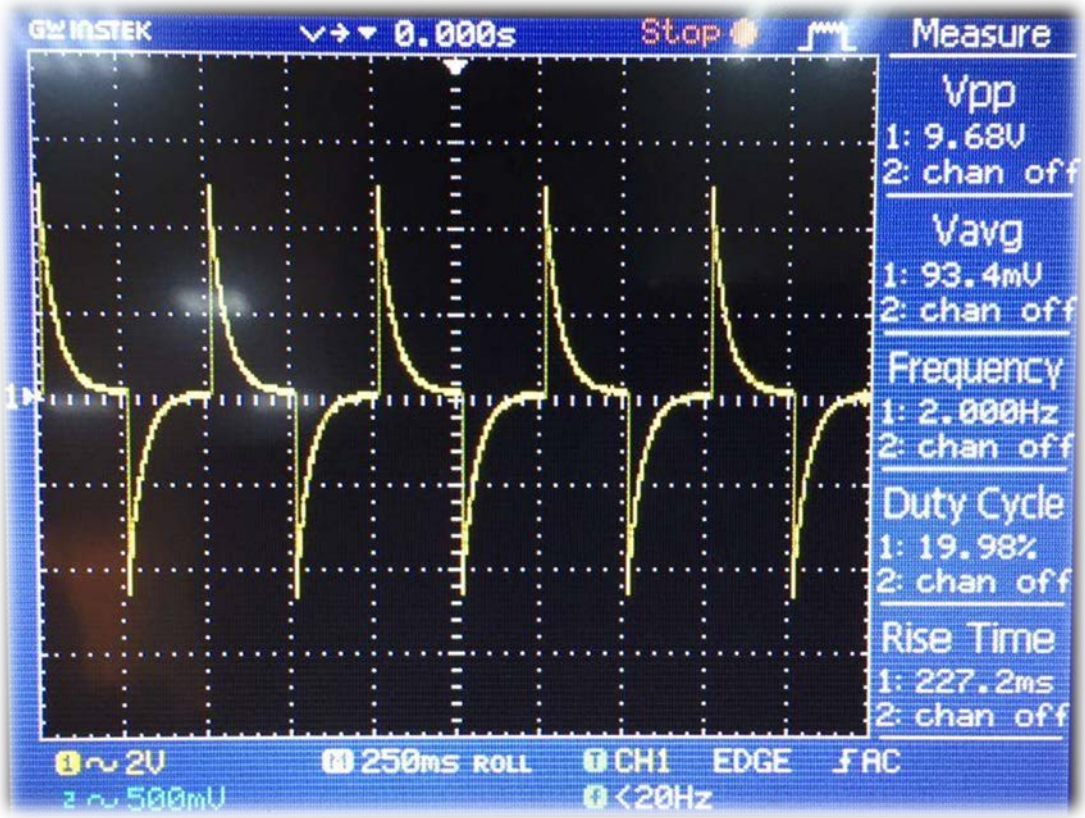


Fig.(4.2) :Reading of out put carry binary counter (4060)IC

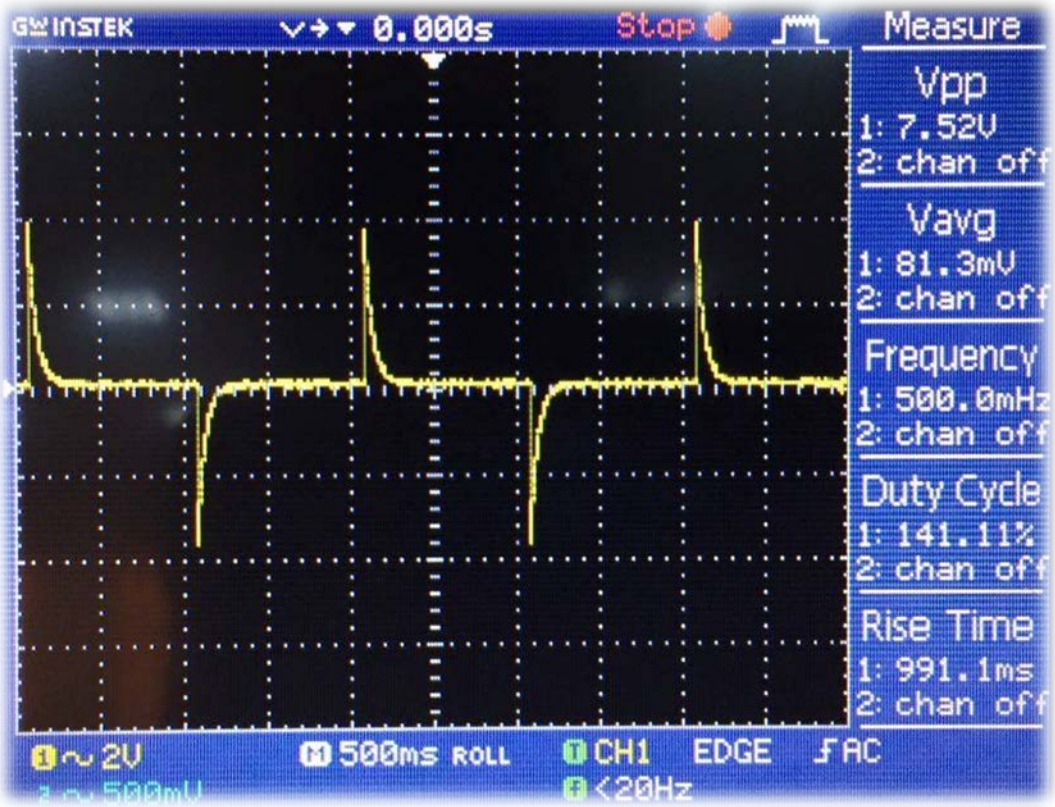


Fig.(4.3) : Reading of out put for frequency divider by using (74170)IC

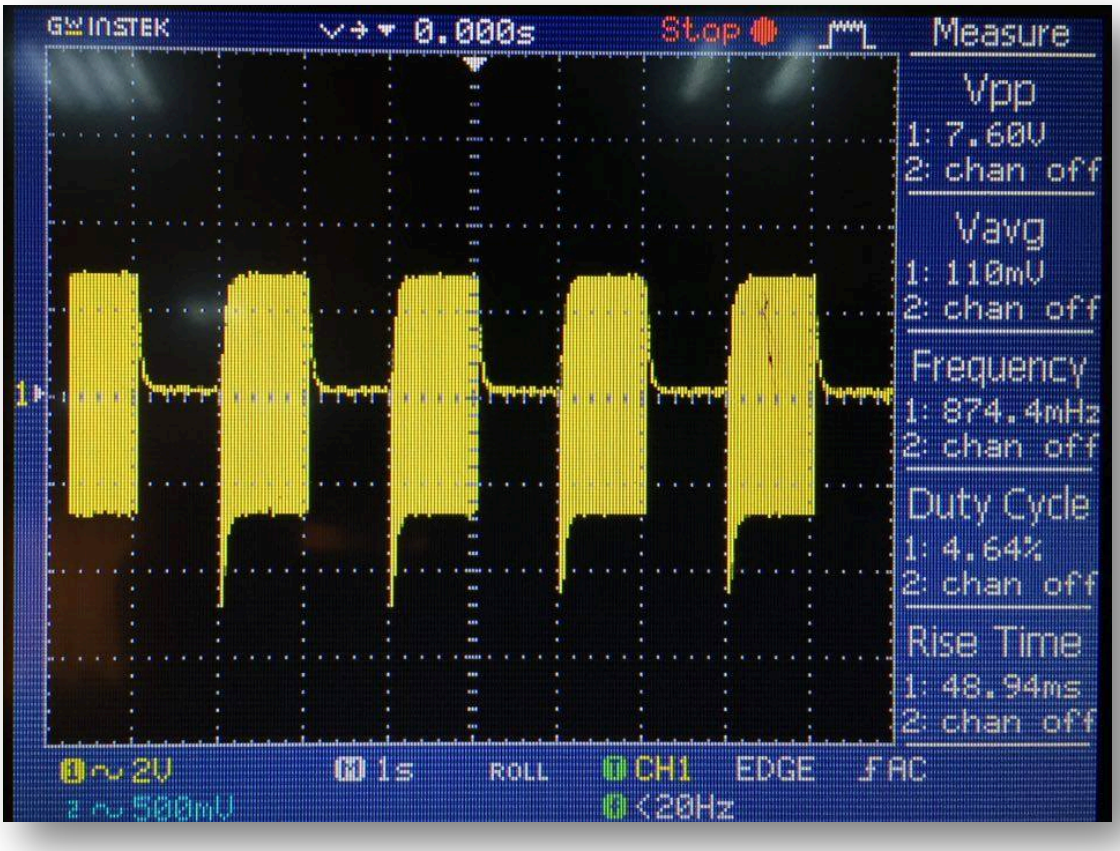


Fig.(4.4) : Reading of out put for 2-input NAND gate by using (4011) IC

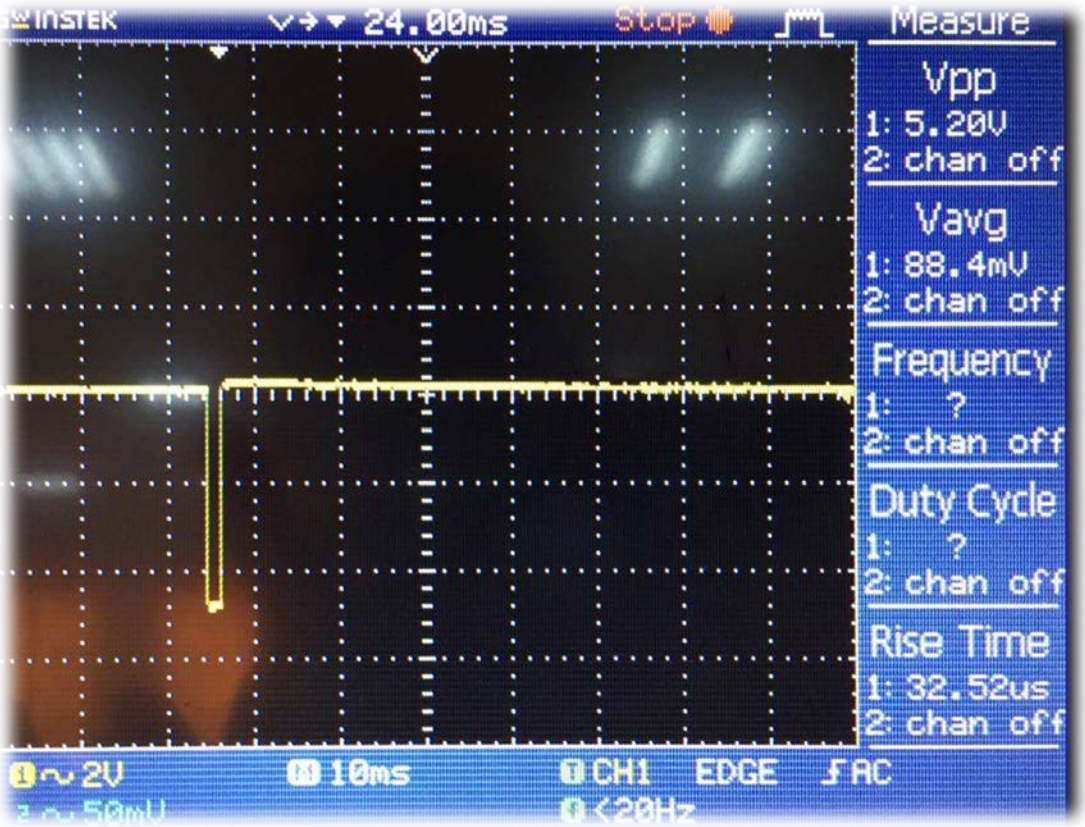
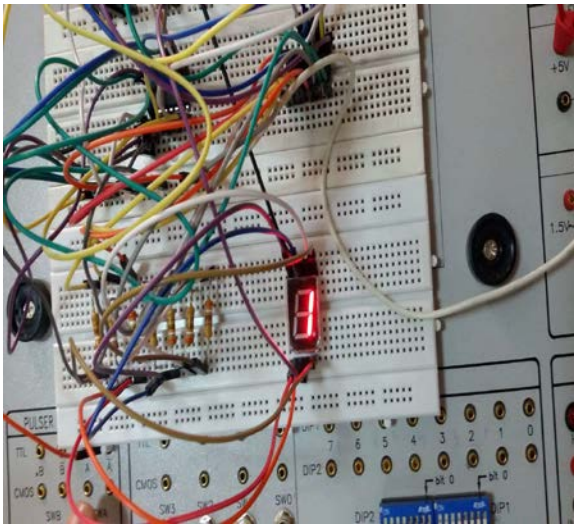


Fig.(4.5) : Reading of out put for 3-digit BCD counter by using (4538) IC

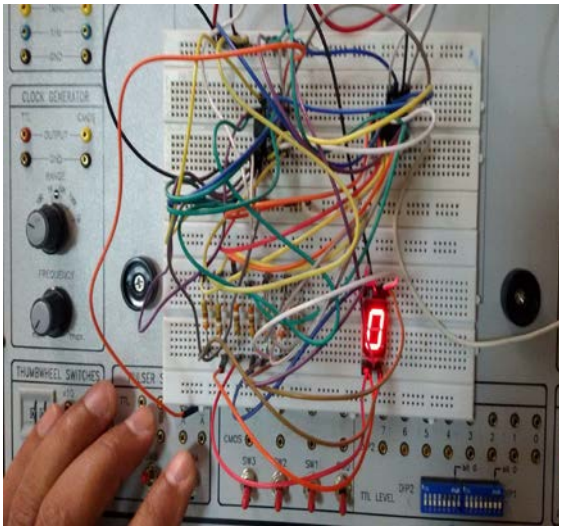
4.2 conclusion

As shown in fig (4.6),Wesaw the digital signal reading, which is easier said than reading device Analog

We can develop the device in the future, up-range frequencies that are read digital device that we have designed and we can also add other components to increase accuracy.



(a)



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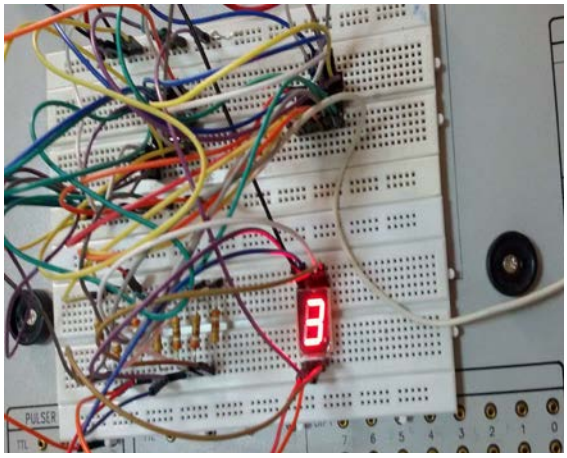
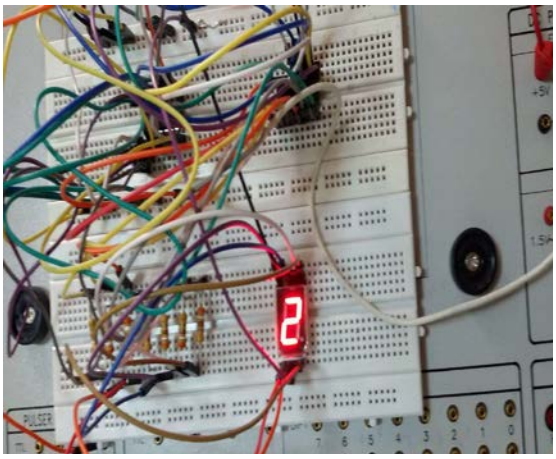


(c)



(d)

Fig.(4.6) : The output of this display

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