Salah Hassan Ibrahim Alkurwy
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Assoc. Prof. PhD in
Department of Electronic Engineering,
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Personal Information

- Nationality: Iraqi
- Date and Place of Birth: 05/ 09 / 1965, Diyala-Iraq
- H index: 5 (based on the researcher's data)
- Address: 32001 Baqubah, Diyala Province, Iraq

Education

- **PhD Degree** in Electronic Engineering, The National University of Malaysia UKM, MY (2015).

Thesis Title: An Area Efficient Read Only Memory (ROM) Design Architecture for High Speed Direct Digital Frequency Synthesizer.

- **M.Sc. Degree** in Electrical-Electronic Engineering, Electro-technic Faculty, University of Belgrade, Serbia. (1989).
- **B.Sc. Degree** in Electrical Engineering, Vazduhoplovna Tehnička Vojna Akademija, Sarajevo, Bosna and Hercegovina. (1986).

Languages

- English , Serbo-Croatian and Arabic

Teaching

- Digital Electronic , Microelectronic
- Digital System Design
- HDL Programing
- Various Electronics Laboratories
- Supervisor for many graduate projects for undergraduate students.

Training Courses and Workshops

- MATLAB-Xilinx Using System Generator Workshop, Shah Alam, MY November 2012.
- Introduction to FPGA Design using Altera, Kualalumpur, MY, December 2012.
- Several workshops during my PhD study at Electrical Electronic and System Engineering, National University of Malaysia UKM, MY, 2011-2015.

Software and Tools

- ALTERA QurtusII & ModelSim Design Suite, MATLAB: Simulink
- Electronics Workbench, Microsoft Office, Word, Excel, Power Point and Access

Work Experiences

- Lecturer of many subjects at Department of Electronic Engineering, College of Engineering, University of Diyala from 2006-till now, such as: (Electronic , Digital Electronic, Microelectronic and HDL programming).

Professional memberships

- Head of the Department of Electronic Engineering,
- Member of the college of engineering council, University of Diyala.
- Experienced Engineer, member of Iraqi Engineer Union

Publications
Journal **:**

No	Title	Journal Name	Issue ,Vol. & Pages
1	Hardware Implementation of 32-Bit High-Speed Direct Digital Frequency Synthesizer",	Scientific World Journal	10.1155/2014/131568
2	12-Bit High Speed Direct Digital Frequency Synthesizer Based On Pipelining Phase Accumulator Design	Journal of Asian Scientific Research	2(11):667-672
3	High Speed Direct Digital Frequency Synthesizer Using a New Phase accumulator	Australian Journal of Basic and Applied Sciences	393-397 (11) 5
4	Implementation of 32-bit High Speed Phase Accumulator For Direct Digital Frequency Synthesizer	Asian Journal of Scientific Research	10.3923/ajsr.2014. 118.124
5	A low power memoryless ROM design architecture for a direct digital frequency synthesizer	Turkish Journal of Electrical Engineering & Computer Sciences	**25 (5), 4023-4032**
6	Design of a high-performance multiplier based on multiplexer	International Journal of Engineering & Technology	**7 (4), 4182-4185**
7	FPGA Implementation of FIR Filter Design Based on Novel Vedic Multiplier	International Review on Modelling and Simulations	12 (2), 66
9	A novel approach of multiplier design based on BCD decoder	Indonesian Journal of Electrical Engineering and Computer Science	14 (1), 38 -42
10	An area efficient memory-less ROM design architecture for direct digital frequency synthesizer	International Journal of Electrical and Computer Engineering	11 (1), 257 -264
11	Design and Implementation of Parallel Multiplier Using Two Split Circuits	Przegląd Elektrotechniczny	07 (04), 19 - 22
12	A novel pipelined carry adder design based on half adder	Indonesian Journal of Electrical Engineering and Computer Science	IAES

Publications:
Conference

No	Conference Name	Title	Publisher
1	IEEE-ICSE2014 Proc. 2014, Kuala Lumpur, Malaysia,	Implementation of Low Power Compressed ROM for Direct Digital Frequency Synthesizer	IEEE
2	IEEE- ICSE2012 Proc. 2012, Kuala Lumpur, Malaysia	High Speed Direct Digital Frequency Synthesizer with Pipelining Phase Accumulator Based on Brent-Kung Adder	IEEE
3	International Synopsion on Instrumentation & Measurement, Sensor Network and Automation (IMSNA), China; 2012	Design A 24-Bits Pipeline Phase Accumulator For Direct Digital Frequency Synthesizer	IEEE

Publications:
Book

No	Book Title	ISBN
1	A Novel ROM Design for High Speed DDFS, LAMBERT Academic Publishing, Germany, 2014.	978-3-659-56639-4

More information about my scientific activity can be found via links below:

Research Gate https://www.researchgate.net/profile/Salah-Alkurwy

Acadimeca.edu https://uodiyala.academia.edu/SalahAlkurwy

Google Scholar https://scholar.google.com/citations?user=c2eG3JMAAAAJ

ORCID ID orcid.org/0000-0002-4495-0046

Publons https://publons.com/researcher/1774228/salah-alkurwy/publications/