Transistor

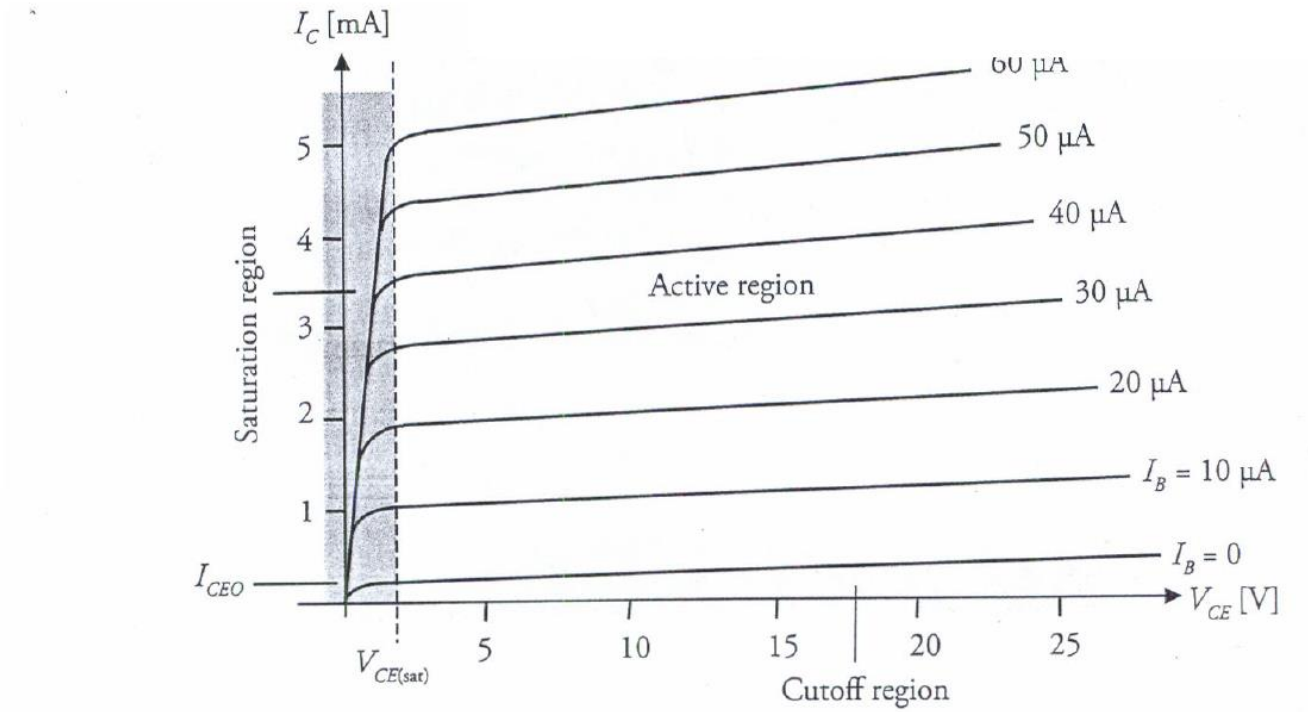

Figure ()
Output characteristics graph for NPN transistor with common emitter configuration.

1-Cutoff Region

To avoid distortion at signals from being amplified, a transistor should not operate in a cutoff region, which is below I_B=0 curve . In this region, both base-emitter and base-collector junctions are in a reverse bias condition.

Look at I_B=0, the collector current, I_c is not zero. At this moment, the value of emitter current is I_{CEO} that flows when a base-collector junction is reverse bias. This can be proven as follows:

$I_E = I_c + I_B$

$I_c = \alpha I_E + I_{CBO}$

$I_c = \alpha(I_C + I_B) + I_{CBO}$

$I_c\,(1-\alpha) = \propto I_B + I_{CBO}$

$I_c = \frac{\propto}{1-\propto} I_B + \frac{I_{CBO}}{1-\propto}$

When I_B=0, hence collector current

$I_c = \frac{I_{CBO}}{1-\propto} = I_{CEO}$

Where α value is $0.90 \leq \alpha \leq 0.99$

2-Saturation Region

I_E and I_C can be too large, when both BE and BC junctions are forward biased. The V_{CE} value at this time is very small (V_{CE} ≈0) . This region should be avoided when a transistor wanted to be used as amplifier; but if the transistor is used as logical switch, it has to be in this region and it said ‘ON’. At this moment, the base is flooded with majority carriers, but the collector voltage is too low to attract all of the majority carriers.

3-Active Region

To enable a transistor functions as an amplifier, with very little distortion, it must be operated in active region. In this region a transistor is in a forward bias condition at the BE junction and reverse bias at the BC junction. An active region is located above the line I_B =0, and the right from V_{CEsat}. The active region is limited to upper part by line I_{Cmax} , this is the maximum value of I_C which can follow at a transistor without damage it, and this value is determined by a manufacture who produces that a transistor. On the right side, it is limited by V_{CEmax} , and is also determined by the manufacture, so the breakdown will not occur. If breakdown happens, there will be an increment of current I_C drastically and it will damage the transistor.

For a common emitter connection, the ratio of small changes of collector current I_C , to a small changes of the base current I_B , with fixed V_{CE} at certain value is called CE forward current gain amplification factor and is known as β_{DC} or β only.

$\beta_{DC} = \frac{I_C}{I_B}$ at fixed V_{CE} or $\beta = \frac{I_C}{I_B}$

I_C and I_B values are in active region. This β value can be obtained from a CE output characteristic graph. Value of β is also known as h_{FE} that is commonly stated in the datasheet.

From equation above, the collector current is $I_C = \beta I_B$. Knowing that

I_E=I_c + I_B , hence I_E= β I_B + I_B or I_E= (1+ β) I_B

The relationship between α and β is α=$\frac{\beta}{\beta+1}$ and β =$\frac{\alpha}{1-\alpha}$

This can be proven as follows:-

α=$\frac{I_C}{I_E}$ $\rightarrow$ I_E = $\frac{I_C}{\alpha}$

β=$\frac{I_C}{I_B}$ $\rightarrow$ I_B = $\frac{I_C}{\beta}$

Then substitute I_E=I_c + I_B

Thus $\frac{Ic}{\alpha}$ = I_c + $\frac{I_c}{\beta}$ or $\frac{1}{\alpha}$ = 1 + $\frac{1}{\beta}$

Simplify $\beta = \alpha\beta + \alpha = \alpha(1+\beta) \rightarrow \alpha = \frac{\beta}{\beta+1}$

Or $\beta - \alpha\beta = \alpha \rightarrow \beta = \frac{\alpha}{1-\alpha}$

Using α and β expressions, the relationship between minority I_c for common base and common emitter connection is:-

$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = (\beta + 1)\, I_{CBO}$

4-Common collector configuration

For this connection, the input signal at the base terminal and output signal can be obtained from the emitter as shown in figure below.

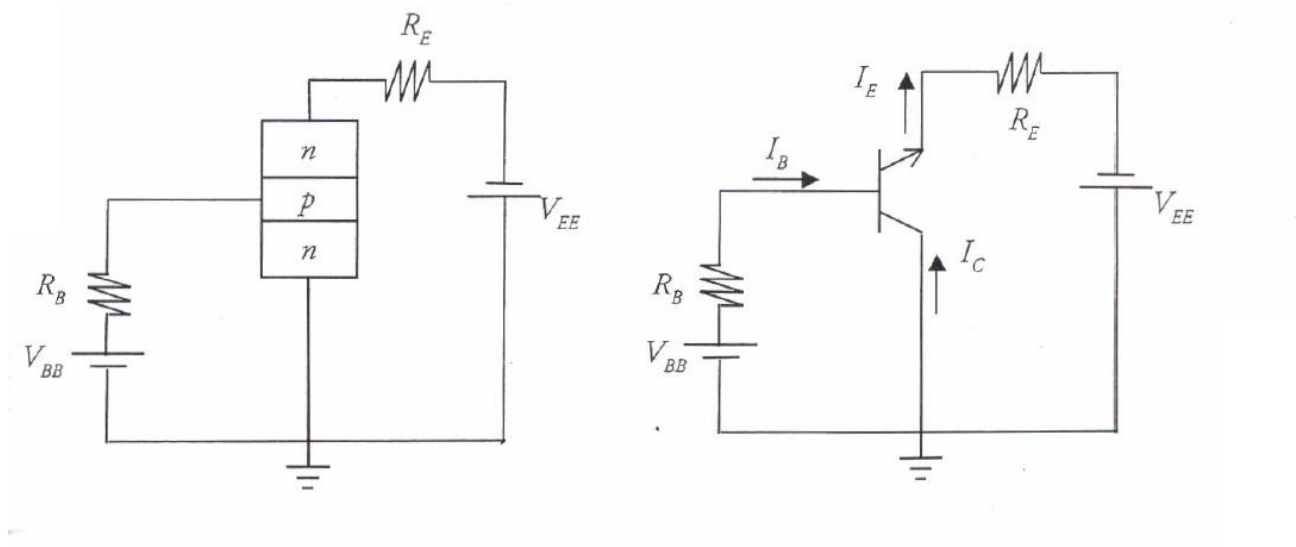

Figure (1)
Common collector connection of an NPN transistor

The output characteristic graph shown in figure (2) is the output characteristic for NPN transistor with a common collector (CC) configuration. As can be seen, the output characteristics for a CC configuration is almost similar to the output characteristics for a CE configuration. All current relationships that have been discussed are used for CC configuration and can be used.

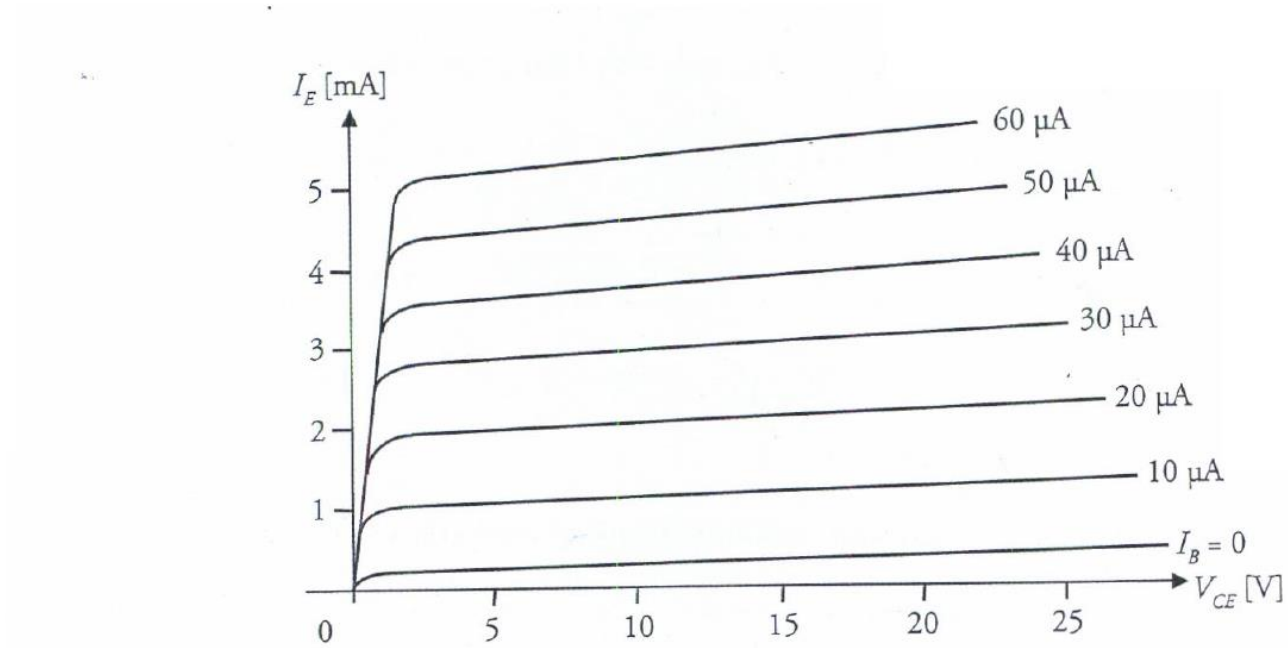

Figure (3)

Output characteristics for a NPN transistor with a common collector configuration

5-Limits of operation

BJT transistor is widely used as an amplifier. Therefore, it is important to know the limits of operation of a transistor. There are at least three maximum values that started in data sheet:

a- Collector maximum power dissipation :P_{Cmax} or P_D

b- Maximum collector voltage: V_{CEmax}

c- Maximum collector current:I_{Cmax}

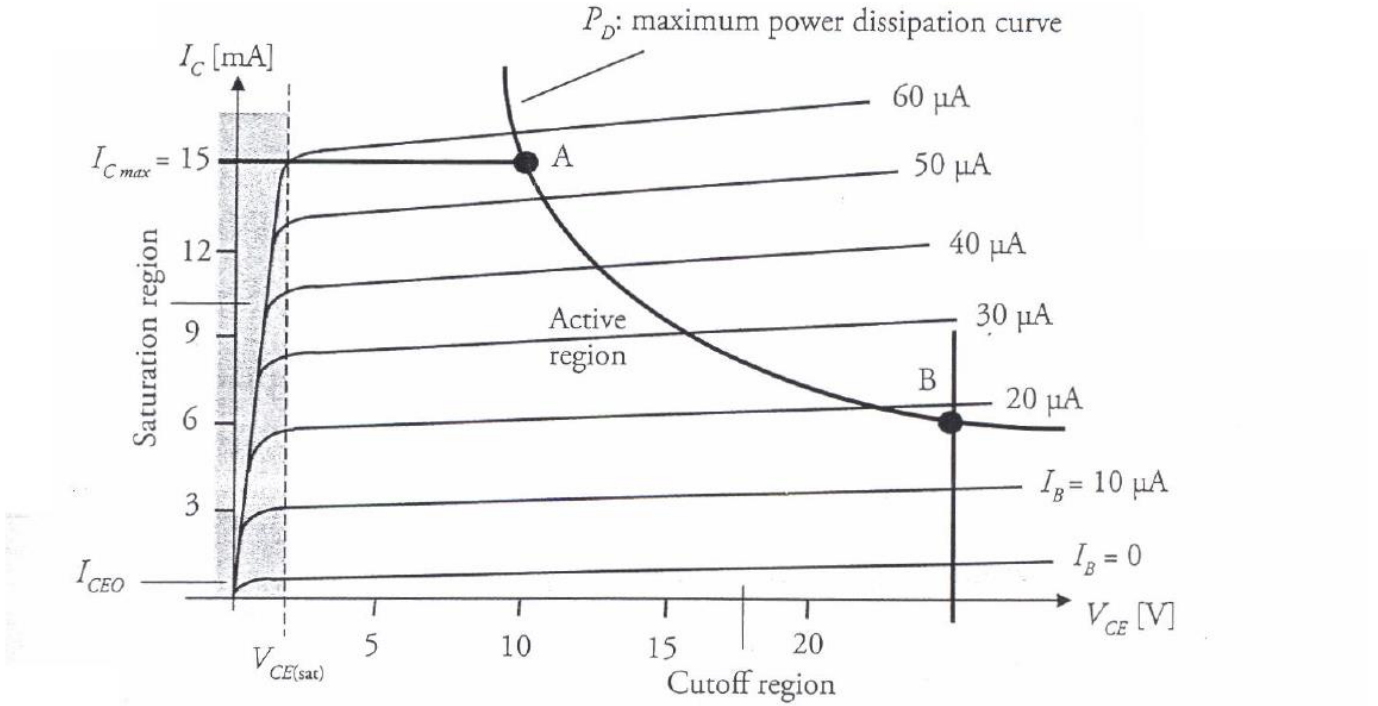

Figure (4)
Operating region of an NPN transistor with a CE configuration

As an amplifier, a transistor should be operated in active mode, not in saturation or cutoff region. A collector current also must not exceed the maximum current allowed, which is I_{Cmax}, and should not exceed the maximum power dissipation determined by the manufactures. V_{CEmax} is the maximum voltage that can be applied across the C and E terminal without damaging the transistor. If V_{CEmax} is over this limit, breakdown will occur: V_{CEmax} is also known as $V_{BR(CEO)}$ or V_{CEO}. Figures (4) shows the operation limit.

Example (1)

From figure (4) , find power dissipated by the transistor.

Solution:-

P_D is obtained as follows:-

Based on figure (4) , I_{Cmax} value for the transistor is 15 mA, while V_{CEmax} is 25 V. If at point A, V_{CE} = 10 V and I_c = 15 mA, hence P_D= V_{CE} x I_c=10 V x 15 mA = 150 mW .

If using point B, P_D=25 V x 6 mA = 150 mW

Thus, the power dissipation or P_D is 150 mW .

Generally, dissipation rate or power dissipation P_D of a transistor with CE connection is given by:

$P_D = P_{Cmax} = P_{CE} \times I_C$

This value is fixed by manufacture and depends on transistor types. For the purpose as an amplifier, a transistor must be operated in an active region under the maximum power dissipation. This curve can be determined using the given equation. To draw this curve, the given P_{Cmax} value is used to find I_C for certain V_{CE} value.

Data sheet gives the maximum power dissipation value at 25° C. If a transistor is used above 25°, the power dissipation value must be derated.

Example (2)

Transistor 2N3904 is used in a circuit with V_{CE}=20 V. This circuit is used at 125° C. Calculate the new maximum I_C value. Given that 2N3904 has maximum power dissipation of 310 mW and must be derated linearly at 2.81 mW / ° C for temperature more than 25 ° C.

Solution:-

Temperature increment = 125° C- 25 ° C= 100 ° C

Power dissipation of transistor = 2.81 mW/ ° C x 100 ° C=281 mW

Maximum power dissipation at 125° C =310 mW -281 mW=29 mW

Therefore: $I_C = \frac{PC_{max}}{V_{CE}} = \frac{29\ mW}{20\ V}$= 1.45 mA

6- DC analysis

BJT should be biased to determine an operating point or Q-point. This is required to ensure whether it is in an active region to be used as an amplifier or in saturation region or cutoff to be used as a switch. BJT bias circuit analysis or also known as DC analysis is done with the aim to determine the operating point.

6-1 Fixed-bias circuit

A fixed-bias circuit is shown in figure (5). The DC analysis of this circuit can be divided into two loops :Input loop and output loop (figure (6)). Currents that flow through every resistor are also shown in this figure.

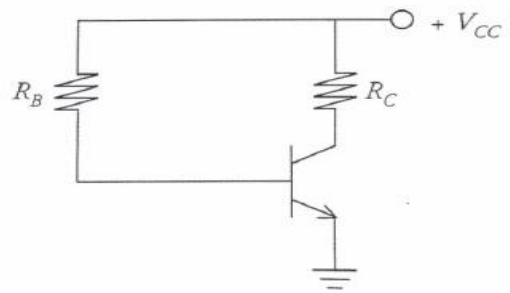

Figure -5- A fixed-bias circuit

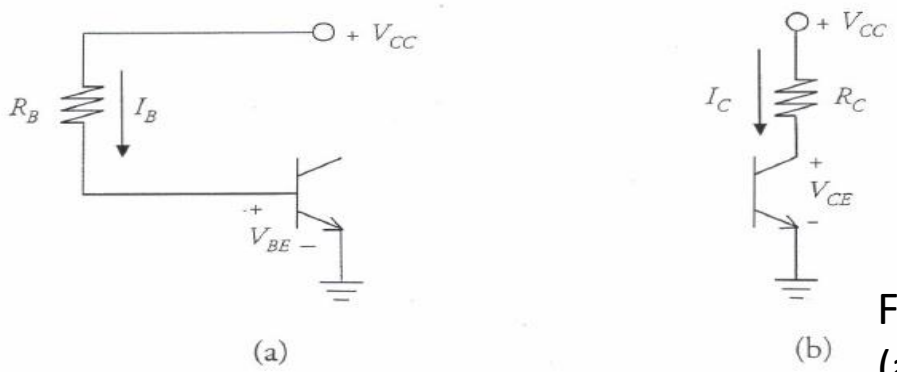

Figure -6- A fixed-bias circuit
(a) Input loop (b) output loop

Using the KVL in the input loop figure (6-a) :-

V_{cc}- $I_B R_B$- V_{BE}=0 $\rightarrow$ $I_B = \frac{V_{cc} - V_{BE}}{R_B}$

Hence $I_c = \beta I_B$

Therefore, emitter current $I_E = I_c + I_B$

Equation for the output loop, figure (6-b):-

V_{cc}- $I_c R_c$- V_{CE}=0 $\rightarrow V_{CE} = V_{cc}$- $I_c R_c$

The I_B, I_c, I_E values obtained show the location of the operating point on the output characteristics graph figure (7). But, in most of the cases, it is sufficient if I_c and V_{CE} values are used, which is the coordinate (V_{CEQ}, I_{cQ}), the Q-point.

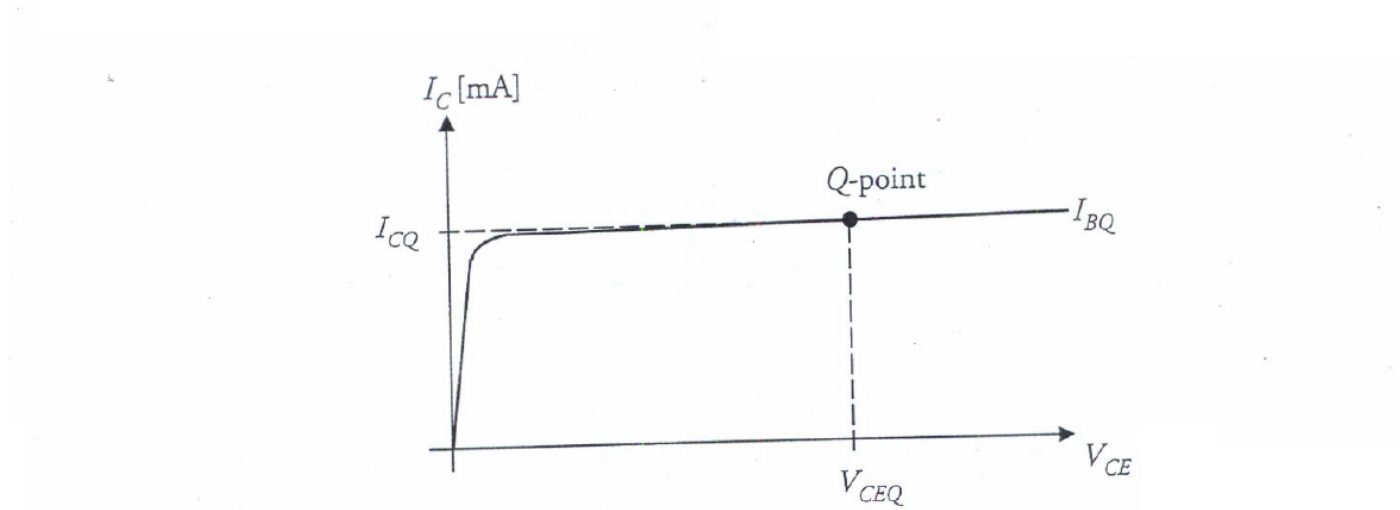

Figure (7)
Location of operating point (Q-point)

6-2 DC Load-line

Using equation from the output loop, one a straight line can be drawn on the output characteristics graph. This line is called DC load-line (DCLL). The operating point or Q-point is always on the DCLL.

From equation V_{cc}- $I_c R_c$- V_{CE}=0, two points on x-axis and y-axis are obtained as follows:-

(1) If I_c= 0 mA, then V_{CE}= V_{CC}= $V_{CE(cutoff)}$ → (V_{CC},0). This point is in the cutoff region.

(2) If V_{CE}= 0 V, then I_c=$\frac{V_{CC}}{R_c}$ = $I_{c(sat)}$ → (0, $\frac{V_{CC}}{R_c}$). This point is in the saturation region.

Using the two points obtained, DCLL is drawn.

Example (2)

A fixed bias circuit shown in figure (5) has the following parameters:

R_c=2 $K\boldsymbol{\Omega}$, R_B=386 $K\boldsymbol{\Omega}$, V_{CC}= 20 V ,V_{BE}= 0.7 V, and β=100. Determine the DCLL.

Solution:-

The DCLL can be obtained as follows:

When I_c= 0 mA, then V_{CE}= V_{CC}=20 V → (20 V,0).

When V_{CE}= 0 V, then I_c= $\frac{V_{cc}}{R_c}$ = $\frac{20\ V}{2K\boldsymbol{\Omega}}$ = 10 mA → (0,10 mA).

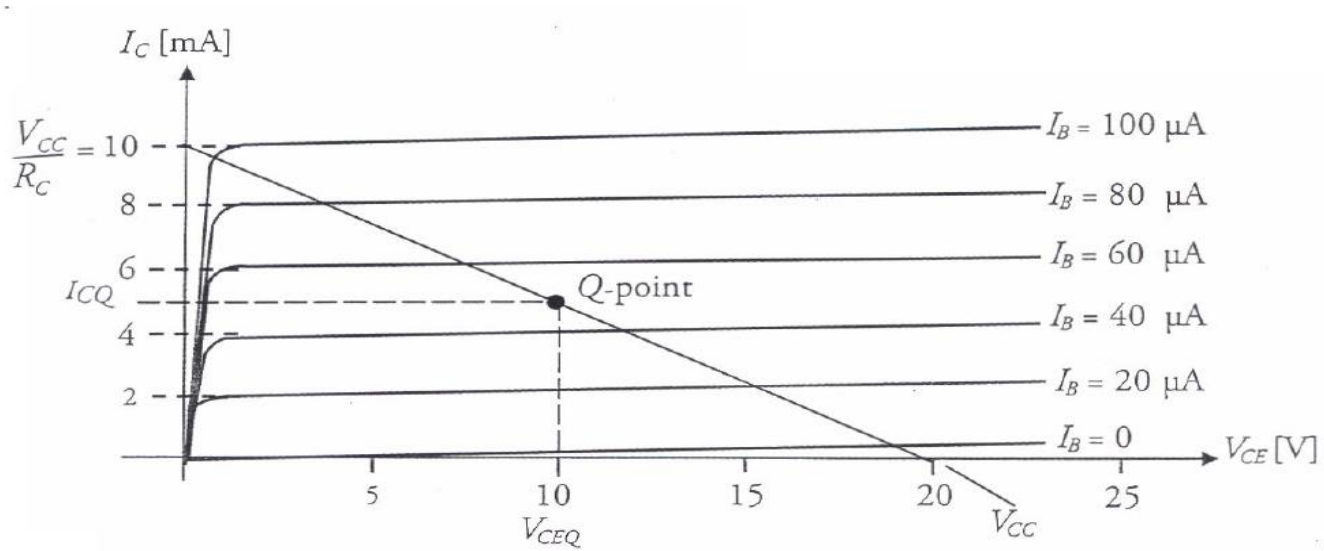

Figure (8)
Load-line for a fixed bias circuit and Q-point

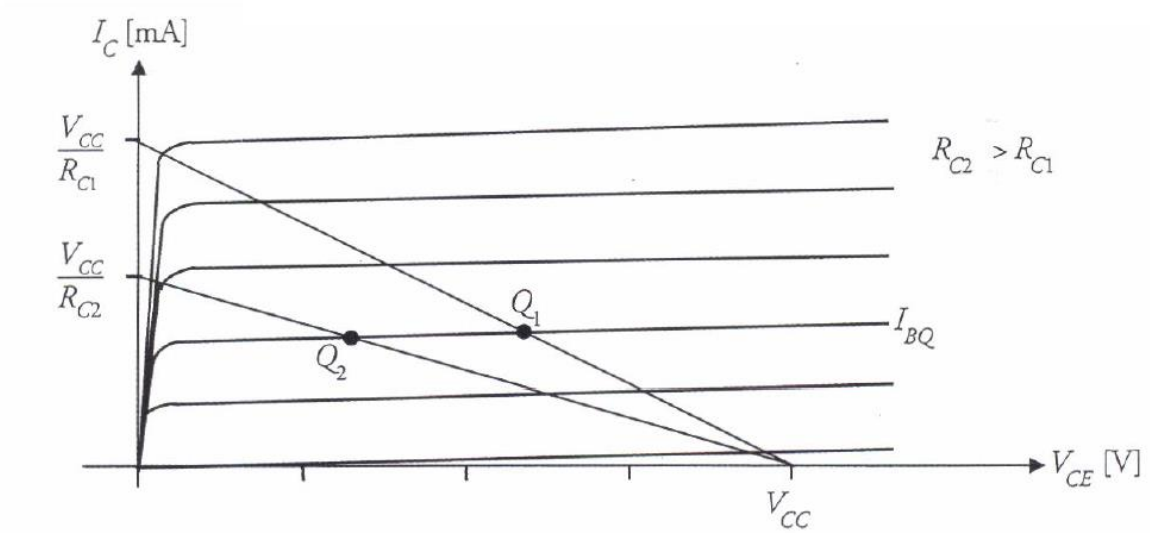

Figure (9)
Effect of changes in R_c and Q-point

Load-line slop depends on the resistor R_c value. If V_{CC} is fixed but R_c changes, the load line slope will change (figure (9)). This causes the operating point to change. Otherwise, the load line slop experiences no change if R_c is fixed but V_{CC} changes figure (10).

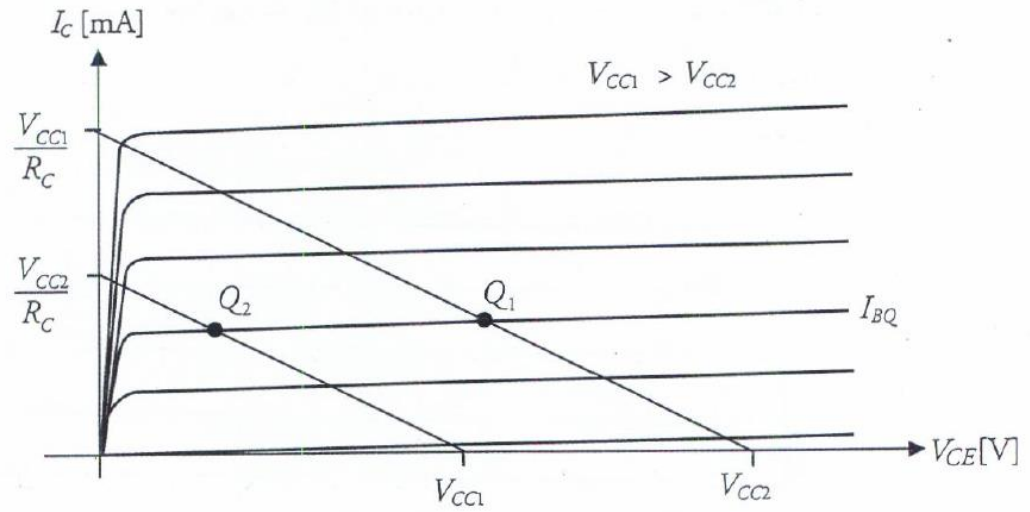

Figure (10)
Effect of V_{CC} value changes at load-line and Q-point : R_c value is fixed

Example (3)

Figure -5- shows a fixed bias circuit and its parameters are: R_c=560 $\boldsymbol{\Omega}$, R_B=100 $K\boldsymbol{\Omega}$, V_{CC}= 12 V, V_{BE} = 0.7 V, and β=100. Determine its operating point and if β is changed to 150. locate the new operating point.

Solution:-

If β=100

I_B=$\frac{12\ V - 0.7\ V}{100\ K\boldsymbol{\Omega}}$ = 113 μA , then I_c =100(113 μA)=11.3 mA

Therefore, V_{CE} =12 V – 11.3 mA(560 $\boldsymbol{\Omega}$)=5.67 V

Hence, the Q-point is (5.67 V, 11.3 mA)

If β=150

I_B=$\frac{12\ V\ -0.7\ V}{100\ K\boldsymbol{\Omega}}$ = 113 μA

I_B value is fixed (does not change with β changes) but I_c will change.

I_c=150 (113 μA)=16.95 mA

Therefore

V_{CE} =12 V – 16.95 mA(560 $\boldsymbol{\Omega}$)=2.51 V

Thus, Q-point is (2.51 V, 16.95 mA)

Percentage of changes:

% Δ I_c=$\frac{16.95m\text{A}\ -11.3m\text{A}}{11.3m\text{A}}$ × 100% = 50 %

% Δ V_{CE}=$\frac{2.51\ V\ -5.67\ V}{5.67m\text{A}}$ × 100% = -55 %

This example reveals that the operating point showed a big change when β change, thus a fixed bias circuit is not stable.