FET Small Signal Analysis

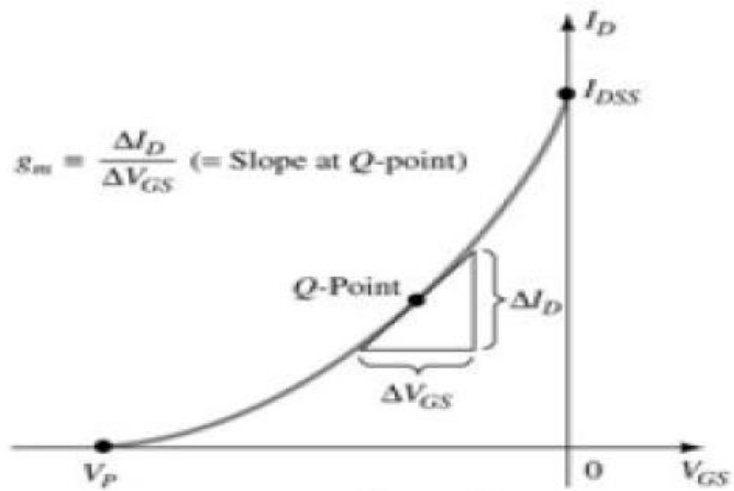
Mathematical Definition of gm

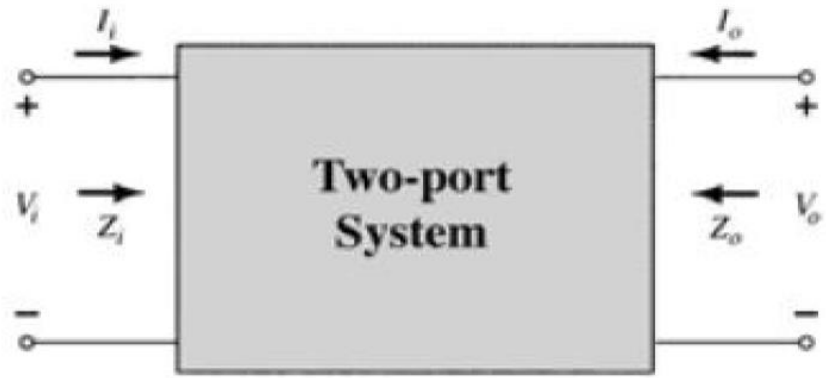
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{GS}} \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

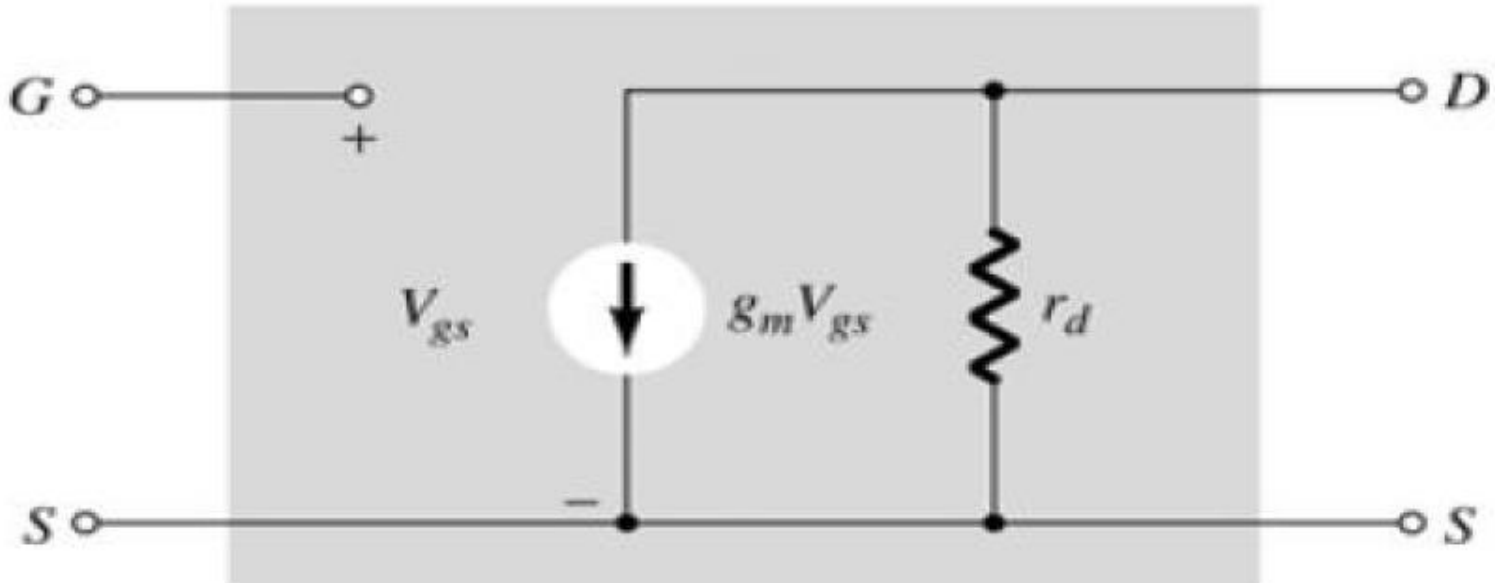
g_m for $V_{GS} = 0V$: $\quad g_{m0} = \frac{2I_{DSS}}{|V_P|}$

for $\quad 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \quad \boxed{g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}}$

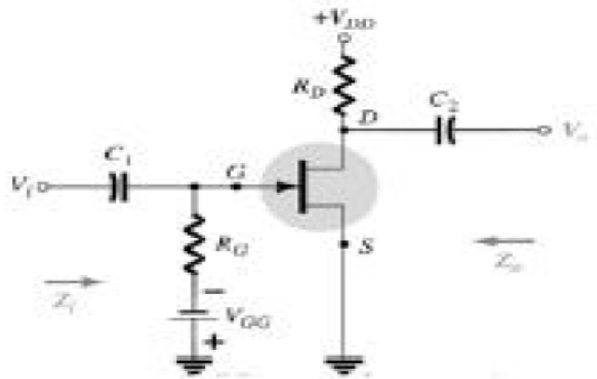

I_D
I_{DSS}
$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ (= Slope at Q-point)
Q-Point
ΔI_D
ΔV_{GS}
V_P
0
V_{GS}



FET AC Equivalent Circuit

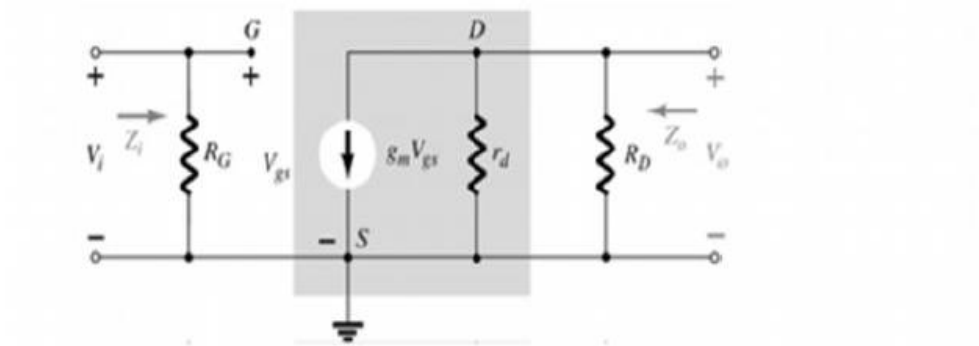

G
+
D
V_{gs}
$g_m V_{gs}$
r_d
−
S
S

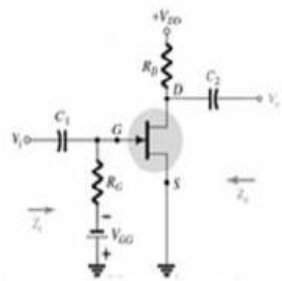
JFET Common-Source (CS) Fixed-Bias Configuration



- The input is on the gate and the output is on the drain.
- Fixed bias configuration includes the coupling capacitors c1 and c2 that isolate the dc biasing arrangements from the applied signal and load.
- They act as short circuit equivalents for the ac analysis.

AC Equivalent Circuit



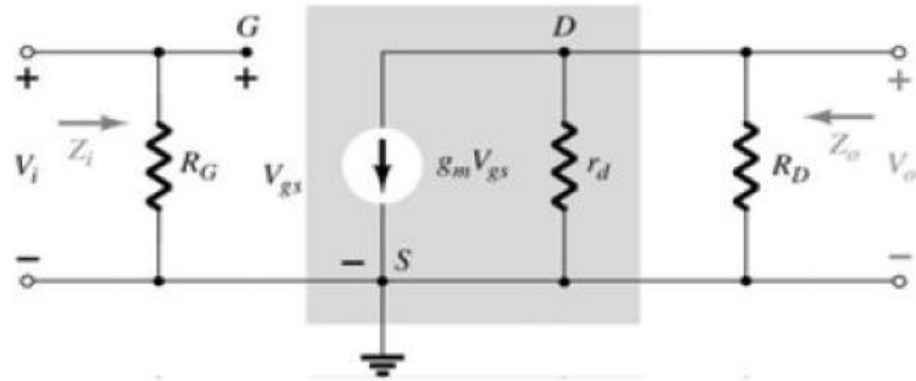


Input impedance $Z_i = R_G$

Output Impedance: $Z_O = r_d \ R_D$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain



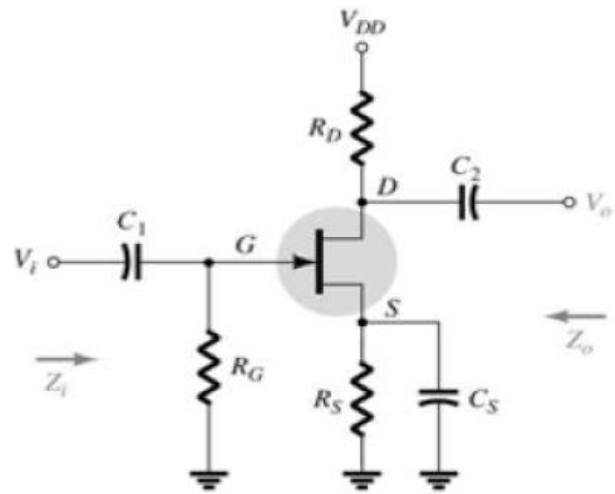
$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10R_D}$$

$$A_v = \frac{V_o}{V_i} = -g_m (r_d \,\|\, R_D)$$

JFET Self bias configuration

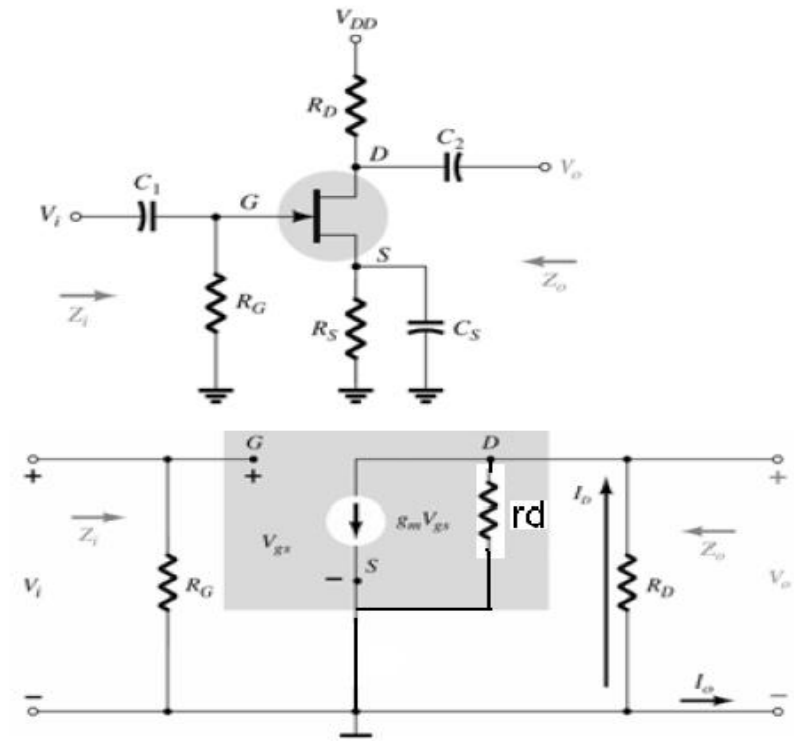
- Main disadvantage of fixed bias configuration requires two dc voltage sources.
- Self bias circuit requires only one DC supply to establish the desired operating point.

Self bias configuration



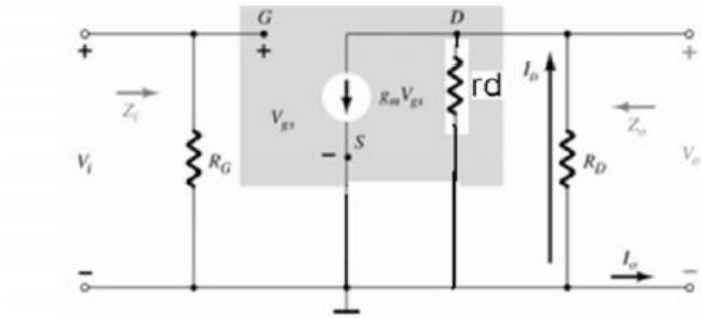
If Cs is removed, it affects the gain of the circuit

AC Equivalent Circuit



- The capacitor across the source resistance assumes its short circuit equivalent for dc allowing RS to define the operating point.
- Under ac conditions the capacitors assumes short circuit state and short circuits the Rs.
- If RS is left un-shorted, then ac gain will be reduced.

Redrawn equivalent circuit:



Here R_s is bypassed by X_{Cs}

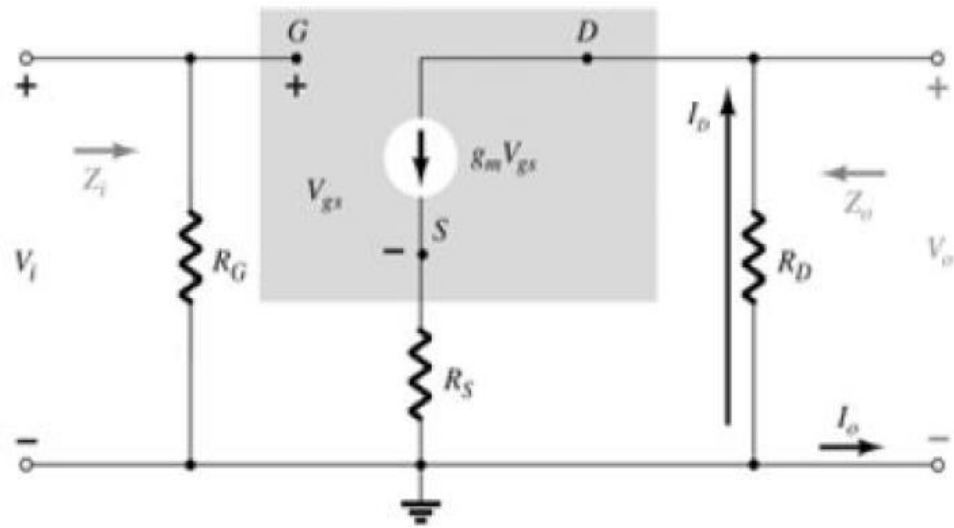
Circuit parameters:

- Since the resulting circuit is same as that of fixed bias configuration, all the parameter expression remains same as evaluated for fixed bias configuration.
- Input impedance Zi=RG
- Output Impedance :Zo= rd parallel RD
- Leaving Rs un-bypassed helps to reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

$$A_v = -g_m(r_d \,||\, R_D)$$

$$A_v = -g_m R_D \,|_{r_d \geq 10R_D}$$

Self bias configuration with un bypassed R_s



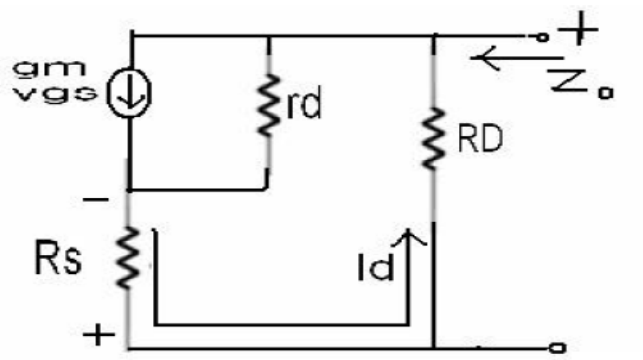
- Here R_s is part of the equivalent circuit .

- Here Rs is part of the equivalent circuit .
- There is no way to reduce the network with lowest complexity.
- Carefully all the parameters have to be calculated by considering all polarities properly.

Output impedance is defined by

- ZO= Vo/Io at vi=0
- Setting Vi=0 results in following circuit

Setting Vi=0 results in following circuit.



$$Zo = \frac{RD}{1 + gmRs + \frac{RD + Rs}{rd}}$$

$$rd > 10(RD + Rs)$$

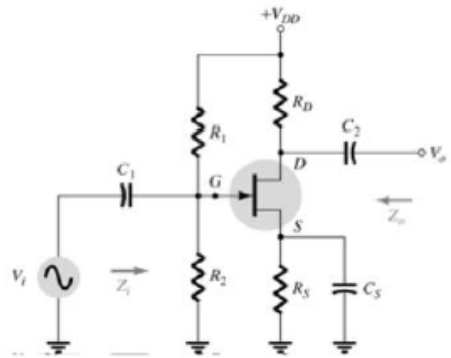
$$Zo = \frac{RD}{1 + gmRs}$$

Voltage gain:

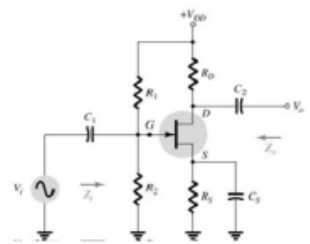
$$Av = \frac{Vo}{Vi} = \frac{gmRD}{1+gmRs+\frac{RD+Rs}{rd}}$$

$$rd \geq 10(RD + Rs), Av = -\frac{gmRD}{1+gmRs}$$

JFET voltage divider configuration



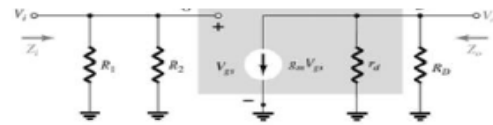
AC equivalent circuit



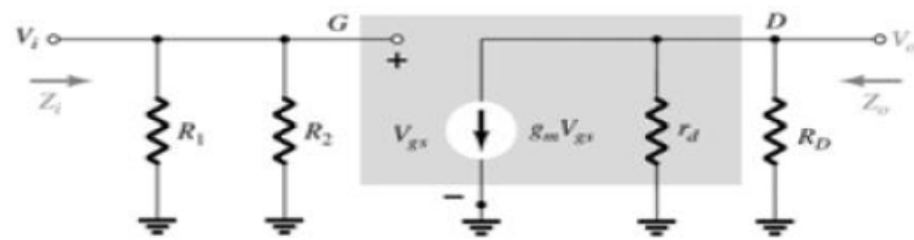
Input Impedance: $Z_i = R_1 \| R_2$

Output Impedance: $Z_o = r_d \| R_D$

$$Z_o \cong R_D \big|_{r_d \geq 10R_D}$$



Voltage gain:



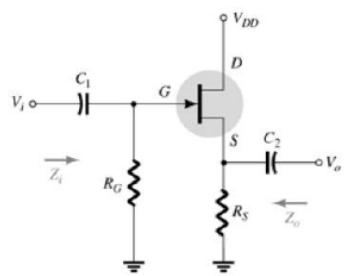
$$A_v = -g_m(r_d \,||\, R_D)$$

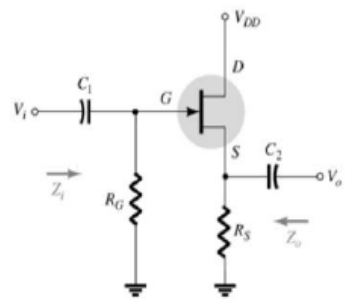
$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

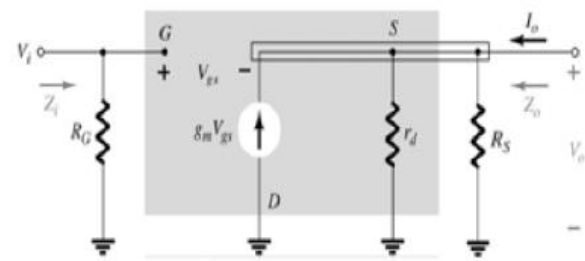
Note

- Equations for ZO and Av are same as in fixed bias.
- Only Zi is now dependent on parallel combination of R1 and R2.

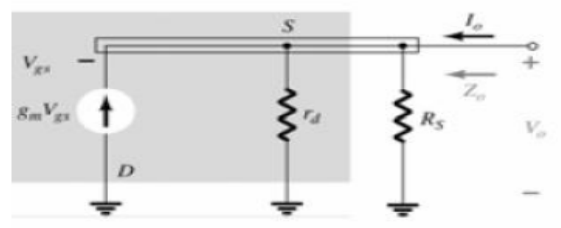
JFET source follower




V_{DD}
D
C_1
G
V_i
S
C_2
V_o
Z_i
R_G
R_S
Z_o


G
S
I_o
V_i
+
V_{gs}
−
Z_i
Z_o
R_G
$g_m V_{gs}$
r_d
R_S
V_o
D
+
−

- Input and output impedance:
- **Input impedance** : Zi=RG
- **Output impedance** :
- setting Vi=0V will result in the gate terminal being connected directly to ground as shown in figure below.



- **Applying KCL at output node**

$$I_o + g_m V_{gs} = I_{rd} + I_{RS}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_s}$$

$$result : I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_s}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_s}\right] - g_m V_{gs}$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{\left[\frac{1}{r_d} + \frac{1}{R_s} + g_m\right]} \frac{1}{V_0}$$

$$= \frac{1}{\left[\frac{1}{r_d} + \frac{1}{R_s} + g_m\right]}$$

$$Z_o \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10R_S}$$

rd, Rs and gm are all in parallel.

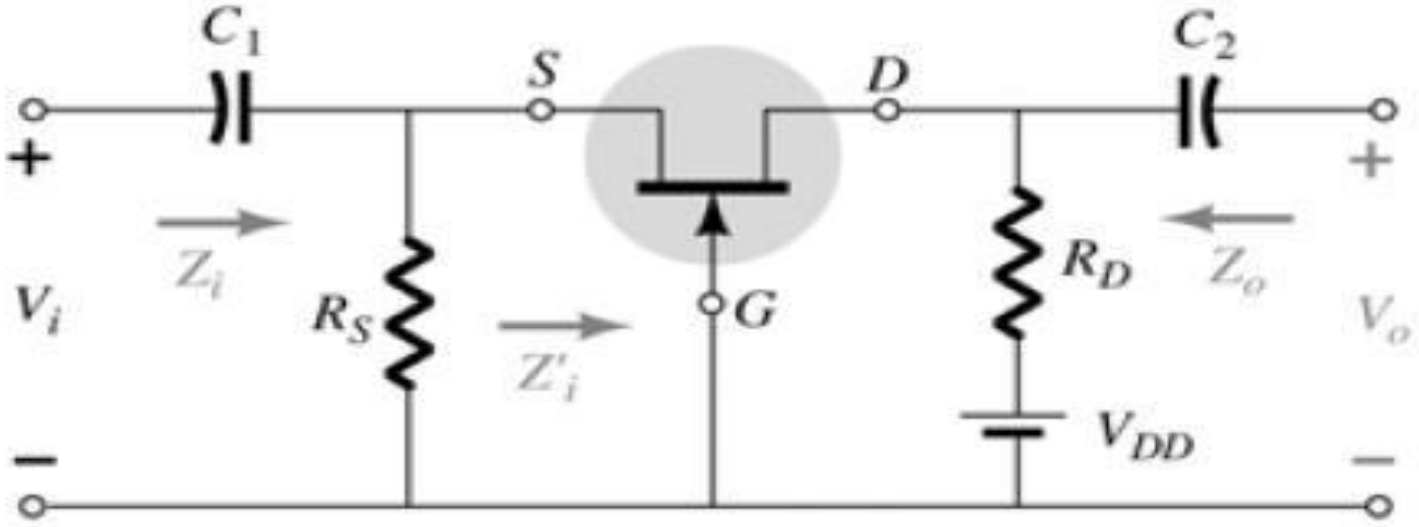
Voltage gain

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$$

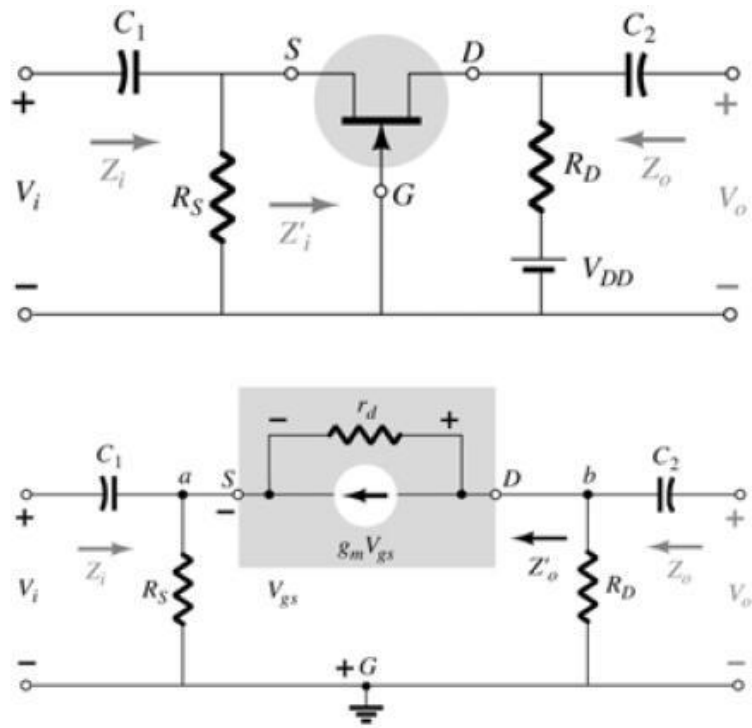
$$A_v = \frac{g_m R_S}{1 + g_m R_S} \Big|_{r_d \geq 10R_S}$$

- Since denominator is larger by a factor of one, the gain can never be equal to or greater than one. (as in the case of emitter follower of BJT)

JFET common gate configuration



- **The input is on source and the output is on the drain. Same as the common base in BJT**

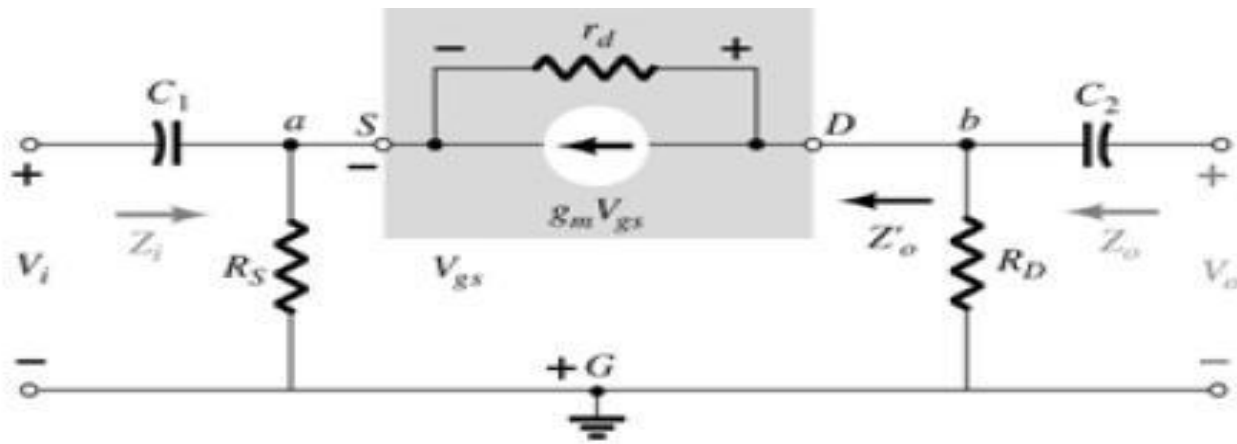


Input Impedance: $Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d} \right]$

$$Z_i \cong R_S \| \frac{1}{g_m} \Big|_{r_d \geq 10R_D}$$

Output Impedance: $Z_o = R_D \| r_d$

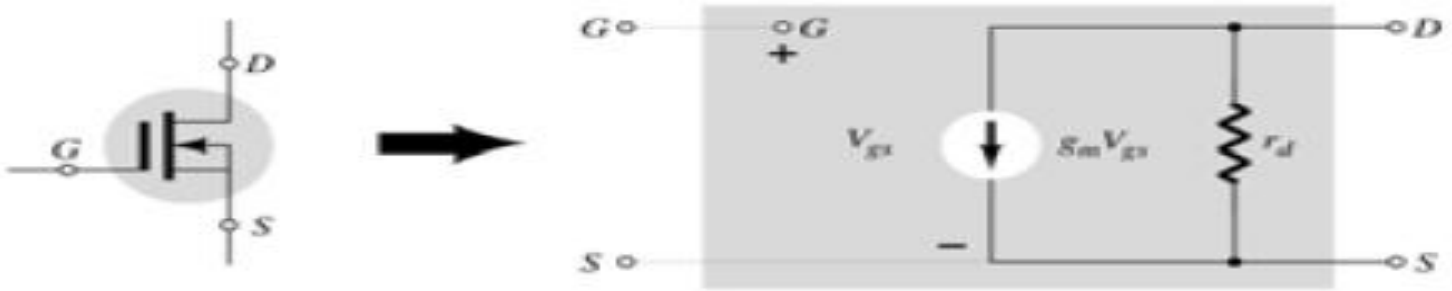
$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



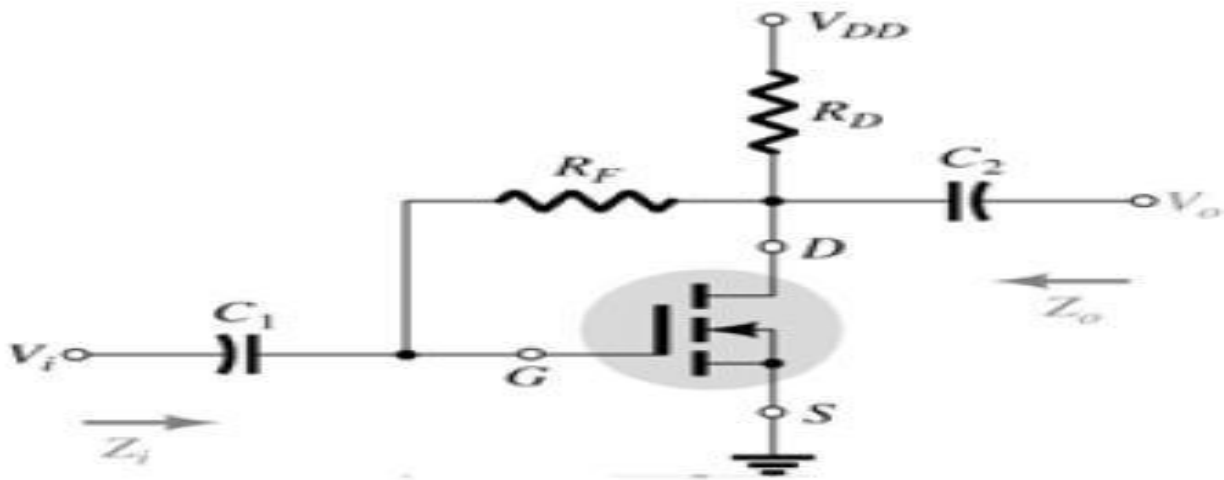
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d} \right]}{\left[1 + \frac{R_D}{r_d} \right]}$$

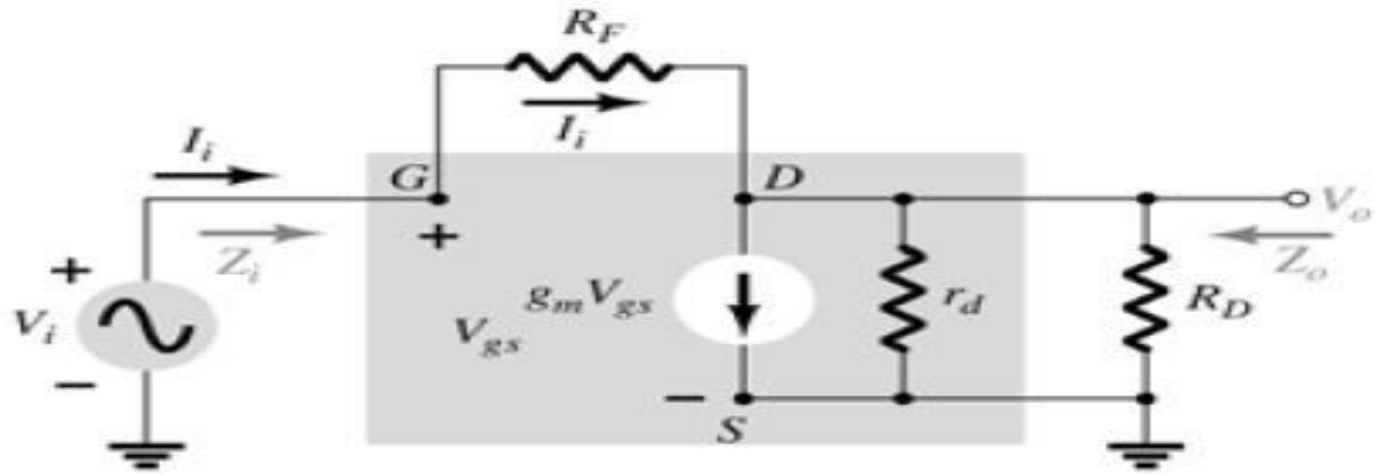
$$A_v = g_m R_D \Big|_{r_d \geq 10 R_D}$$

D-MOSFET ac equivalent model



EMOSFET drain feedback configuration



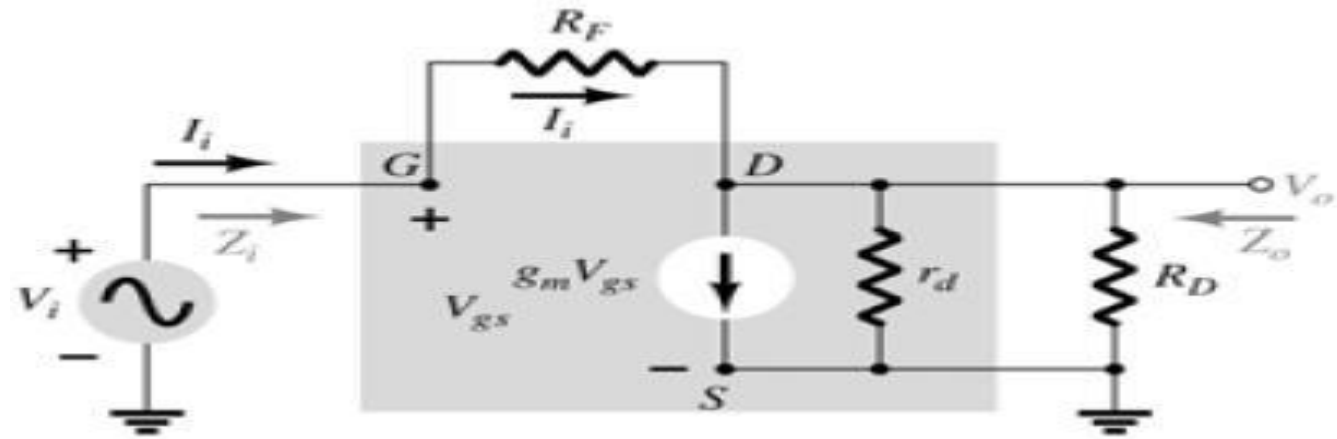

R_F
I_i
I_i
G
D
V_o
Z_i
+
Z_o
+
V_i
$g_m V_{gs}$
r_d
R_D
V_{gs}
−
S
−

Input Impedance: $$Z_i = \frac{R_F + r_d \parallel R_D}{1 + g_m (r_d \parallel R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \Bigg|_{R_F \gg r_d \parallel R_D,\ r_d \geq 10 R_D}$$

Output Impedance: $$Z_o = R_F \parallel r_d \parallel R_D$$

$$Z_o \cong R_D \Big|_{R_F \gg r_d \parallel R_D,\ r_d \geq 10 R_D}$$

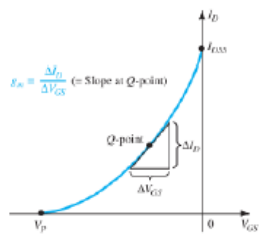


$$A_v = -g_m(R_F \parallel r_d \parallel R_D)$$

$$A_v \cong -g_m R_D\big|_{R_F \gg r_d \parallel R_D,\ r_d \geq 10R_D}$$

JFET small signal Model

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$



$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

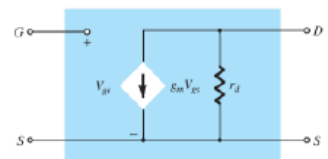


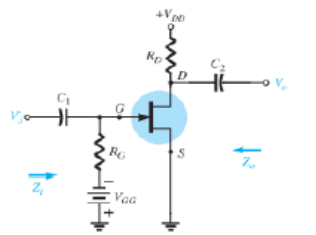
FIG. 8.8
JFET ac equivalent circuit.

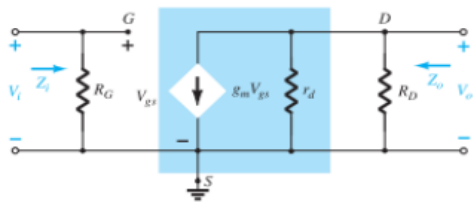
$$Z_i\,(\text{JFET}) = \infty\,\Omega$$

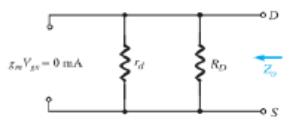
$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

Fixed-Bias Configuration







$$Z_i = R_G$$

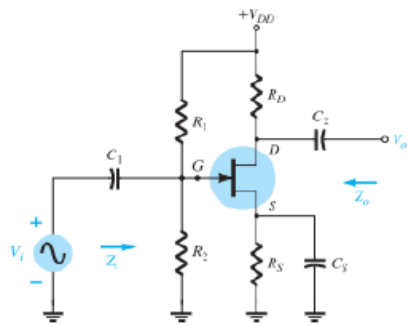
$$Z_o = R_D \| r_d \qquad Z_o \cong R_D \quad r_d \geq 10R_D$$

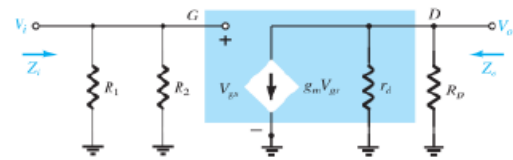
$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d = 10R_D$$

phase shift of 180° between input and output voltages.

VOLTAGE-DIVIDER CONFIGURATION





$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \qquad r_d \geq 10R_D$$

Design FET Amplifier Network

EXAMPLE 8.14 Choose the values of R_D and R_S for the network of Fig. 8.44 that will result in a gain of 8 using a relatively high level of g_{fs} for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

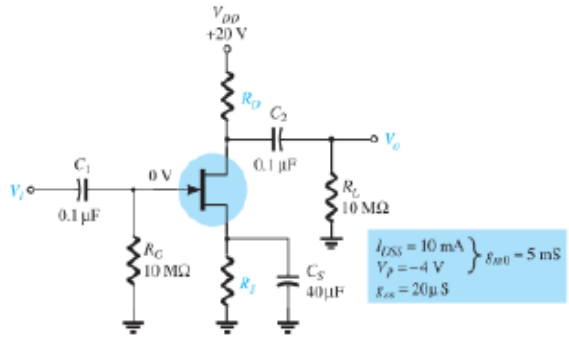


FIG. 8.44
Network for desired voltage gain in Example 8.14.

Solution: The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

and
$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

Determining g_{fs}, we obtain

$$g_{fs} = g_{fs0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$
$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_{fs}(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

so that
$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

and
$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

with the result that

$$R_D = 2.2\text{ k}\Omega$$

which is a standard value.

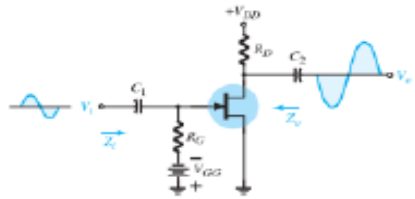
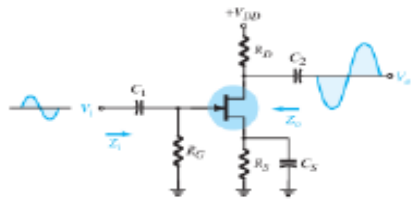
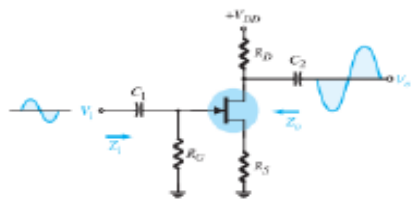
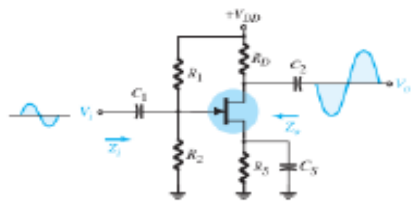
The level of R_S is determined by the dc operating conditions as follows:

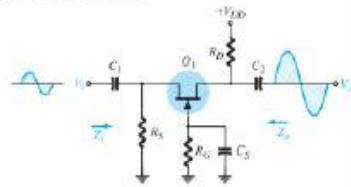
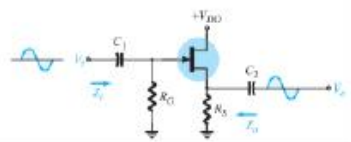
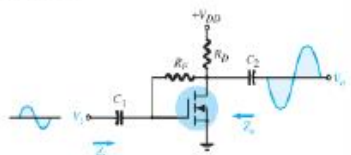
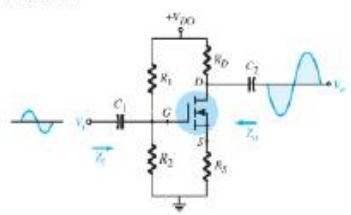
$$V_{GS_Q} = -I_D R_S$$
$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and
$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is **180 Ω**. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

Summary Table

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$	Low (−2) $= \frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\cong \frac{g_m R_D}{1 + g_m R_S}$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \Vert \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$ $\cong R_S \Vert \frac{1}{g_m}$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \Vert R_S \Vert 1/g_m$ $\cong R_S \Vert 1/g_m$	Low (<1) $= \frac{g_m(r_d \Vert R_S)}{1 + g_m(r_d \Vert R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \Vert R_D}{1 + g_m(r_d \Vert R_D)}$ $\cong \frac{R_F}{1 + g_m R_D}$	Medium (2 kΩ) $= R_F \Vert r_d \Vert R_D$ $\cong R_D$	Medium (−10) $= -g_m(R_F \Vert r_d \Vert R_D)$ $\cong -g_m R_D$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \Vert R_2$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$	Medium (−10) $= -g_m(r_d \Vert R_D)$ $\cong -g_m R_D$

Cascaded Configuration

$$A_v = A_{v_1}A_{v_2} = (-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2}) = g_{m_1}g_{m_2}R_{D_1}R_{D_2}$$