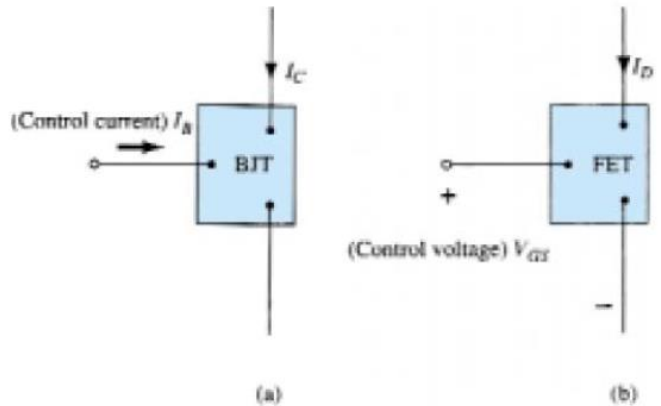
FET (Field Effect Transistor)

- The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor.
- Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow.
- The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig. 1a, while the JFET transistor is a *voltage-controlled* device as shown in Fig. 1b. In other words, the current *IC* in Fig. 1a is a direct function of the level of *IB*. For the FET the current *I* will be a function of the voltage *VGS* applied to the input circuit as shown in Fig. 1b.



(a) Current-controlled and (b) voltage-controlled amplifiers.

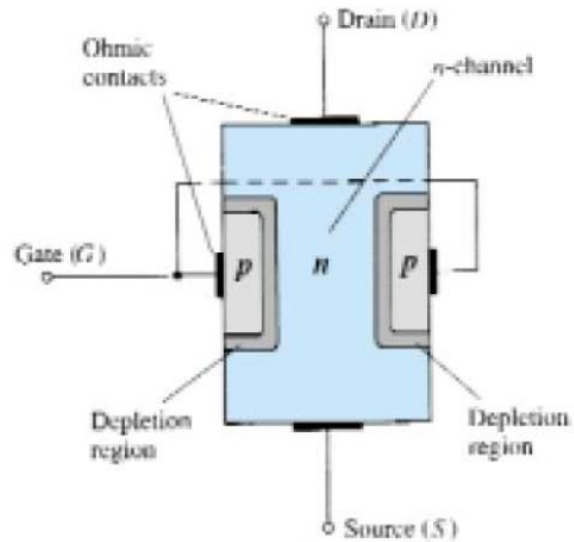
Figure (1)

- Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi-* revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.
- For the FET an *electric field* is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.
- Two types of FETs will be introduced in this chapter: the ***junction field-effect transistor*** (JFET) and the ***metal-oxide-semiconductor field-effect transistor*** *(MOSFET).* The MOSFET category is further broken down into depletion and enhancement types, which are both described.

- The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

Construction AND CHARACTERISTICS OF JFETs:-

- As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two.
- The basic construction of the *n*-channel JFET is shown in Fig. 2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal.



Junction field-effect transistor (JFET).

Figure (2)

- In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p*-*n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 2 that resembles the same region of a diode under no bias conditions. Recall also that a depletion region is that region void of free carriers and therefore unable to support conduction through the region.

- In Fig. 3, a positive voltage *VDS* has been applied across the channel and the gate has been connected directly to the source to establish the condition *VGS* = 0 V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 2. The instant the voltage *VDD* (= *VDS*) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current *ID* with the defined direction of Fig. 3. The path of charge flow clearly reveals that the drain and source currents are equivalent (*ID* = *IS*). Under the conditions appearing in Fig. 3, the flow of charge is relatively uninhibited and limited solely by the resistance of the *n*-channel between drain and source.

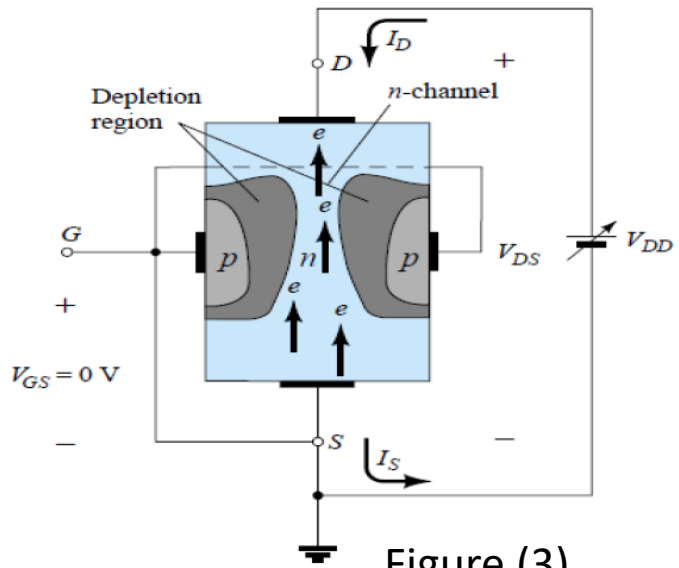
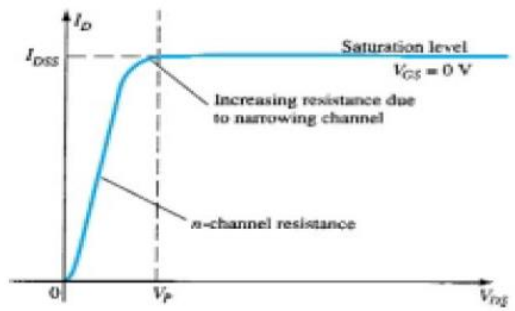


Figure (3)

JFET in the $V_{GS} =$ 0 V and $V_{DS} > 0$ V.

- As the voltage *VDS* is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of *ID* versus *VDS* will appear as shown in Fig. 4 The relative straightness of the plot reveals that for the region of low values of *VDS*, the resistance is essentially constant. As *VDS* increases and approaches a level referred to as *VP* in Fig. 4, the depletion regions of Fig. 3 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 4 to occur.



I_D versus V_{DS} for $V_{GS} = 0$ V.

Figure (4)

- If *VDS* is increased to a level where it appears that the two depletion regions would “touch” as shown in Fig. 5, a condition referred to as *pinch-off* will result. The level of *VDS* that establishes this condition is referred to as the *pinch-off voltage* and is denoted by *VP* as shown in Fig. 4. In actuality, the term *pinch-off* is a misnomer in that it suggests the current *ID* is pinched off and drops to 0 A.

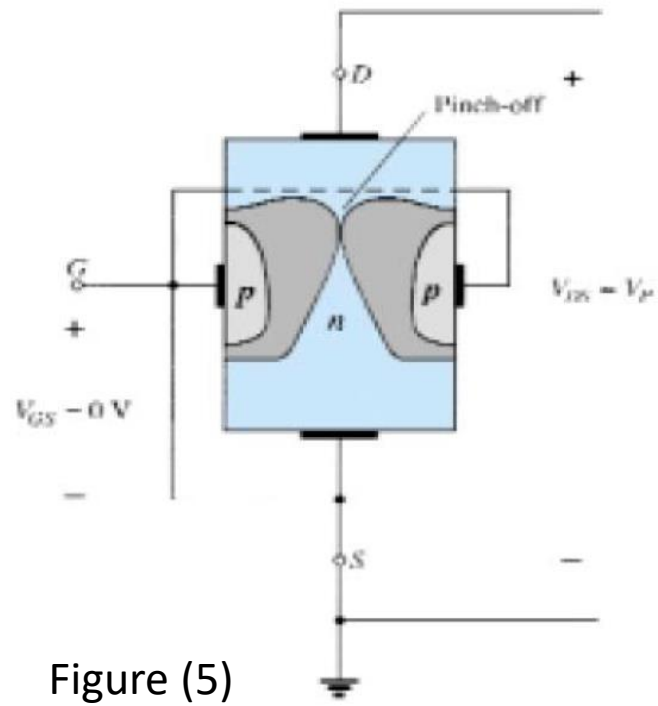
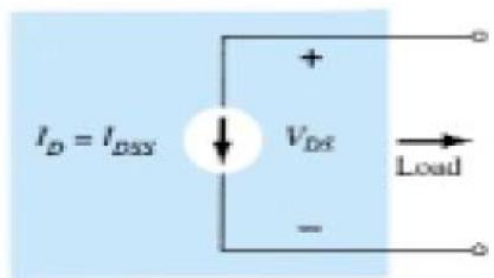


Figure (5)

- As *VDS* is increased beyond *VP*, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of *ID* remains essentially the same. In essence, therefore, once $VDS > VP$ the JFET has the characteristics of a current source. As shown in Fig. 6, the current is fixed at $ID = IDSS$, but the voltage *VDS* (for levels $>VP$) is determined by the applied load.



Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

Figure (6)

IDSS is the maximum drain current for a JFET and is defined by the conditions VGS = 0 V and VDS > |VP|.

VGS > 0 V:-

- The voltage from gate to source, denoted *VGS*, is the controlling voltage of the JFET. Just as various curves for *IC* versus *VCE* were established for different levels of *IB* for the BJT transistor, curves of *ID* versus *VDS* for various levels of *VGS* can be developed for the JFET. For the *n*-channel device the controlling voltage *VGS* is made more and more negative from its *VGS* = 0 V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.
- In Fig. 7 a negative voltage of -1 V has been applied between the gate and source terminals for a low level of *VDS*. The effect of the applied negative-bias *VGS* is to establish depletion regions similar to those obtained with *VGS* = 0 V but at lower levels of *VDS*.

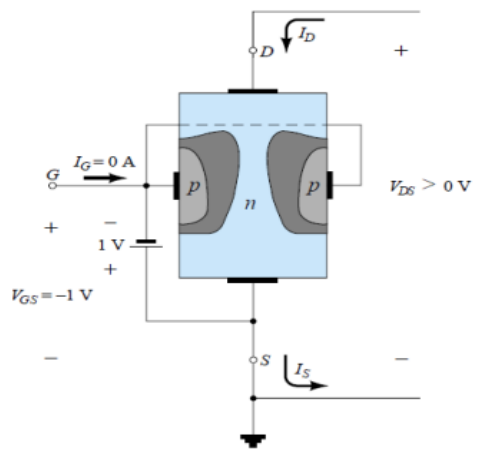
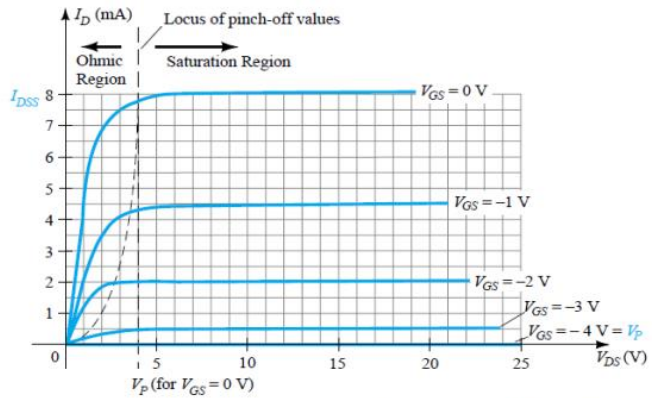


Figure (7)

Application of a negative voltage to the gate of a JFET.

Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of *VDS* as shown in Fig. 8 for *VGS*= -1 V. The resulting saturation level for *ID* has been reduced and in fact will continue to decrease as *VGS* is made more and more negative.



n-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

Figure (8)

- Note also on Fig. 8 how the pinch off voltage continues to drop in a parabolic manner as *VGS* becomes more and more negative. Eventually, *VGS* when *VGS*= -*VP* will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been “turned off.”
- In summary: The level of VGS that results in ID = 0 mA is defined by VGS = VP, with VP being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.
- The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 2, but with a reversal of the *p*- and *n*-type materials as shown in Fig. 9.

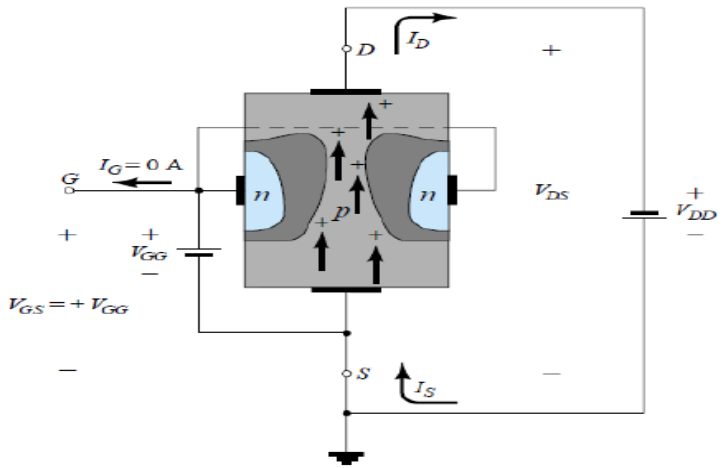
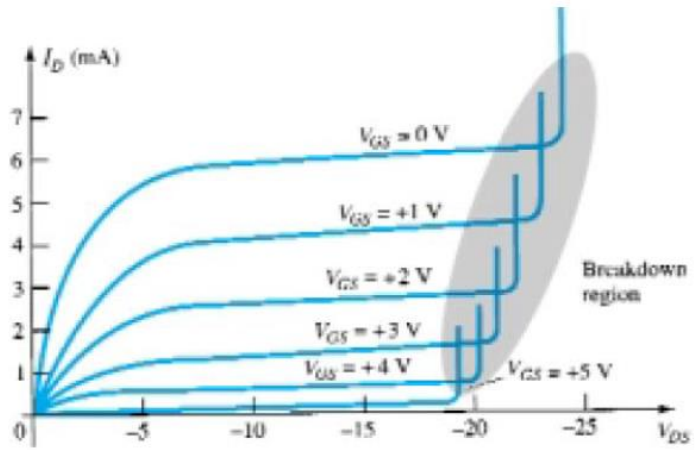


Figure (9)

p-Channel JFET.

- The defined current directions are reversed, as are the actual polarities for the voltages *VGS* and *VDS*. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for *VDS* will result in negative voltages for *VDS* on the characteristics of Fig. 10, which has an *IDSS* of 6 mA and a pinch-off voltage of *VGS*= + 6 V. Do not let the minus signs for *VDS* confuse you. They simply indicate that the source is at a higher potential than the drain.



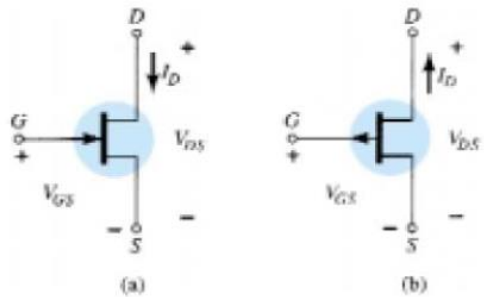
p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Figure (10)

- Note at high levels of *VDS* that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit.

Symbols:

- The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 11 Note that the arrow is pointing in for the *n*-channel device of Fig. 11a to represent the direction in which *IG* would flow if the *p*-*n* junction were forward-biased. For the *p* channel device (Fig. 11b) the only difference in the symbol is the direction of the arrow.



JFET symbols: (a) *n*-channel; (b) *p*-channel.

Figure (11)

- Summary:-
- The maximum current is defined as IDSS and occurs when VGS = 0 V and VDS ≥ |VP| as shown in Fig. 12a.
- For gate-to-source voltages VGS less than (more negative than) the pinch-off level, the drain current is 0 A (ID = 0 A) as appearing in Fig. 12b.
- For all levels of VGS between 0 V and the pinch-off level, the current ID will range between IDSS and 0 A, respectively, as reviewed by Fig. 12c.
- For p-channel JFETs a similar list can be developed.

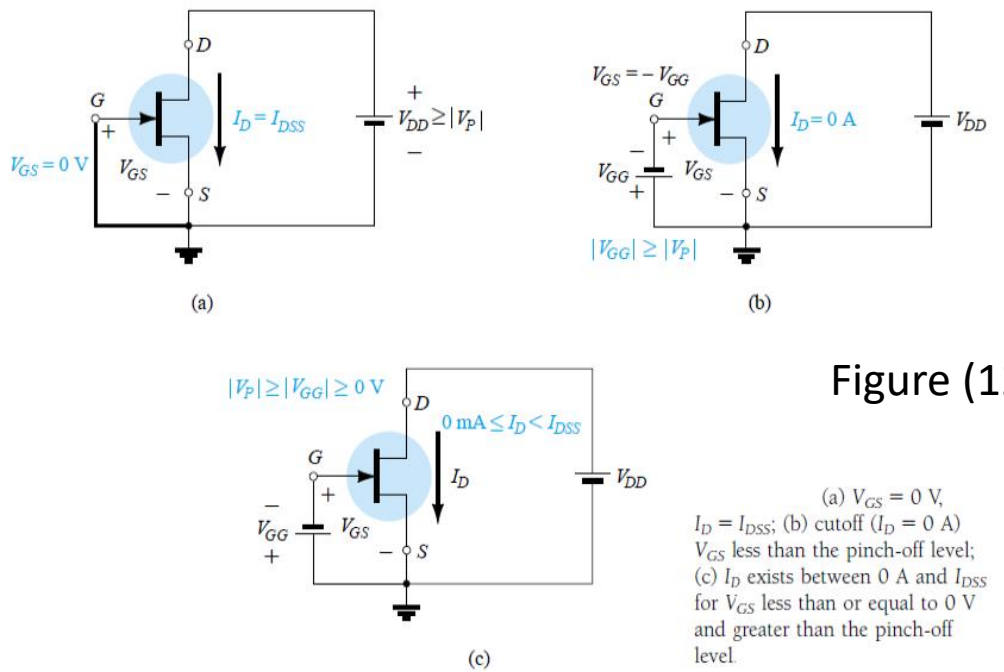
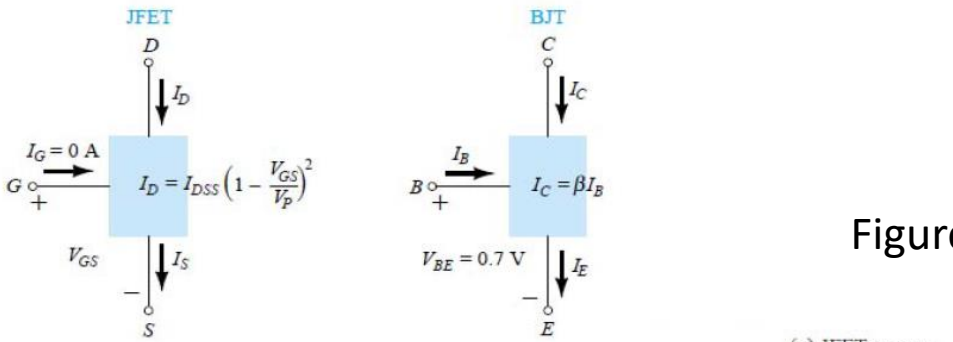


Figure (12)

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.

IMPORTANT RELATIONSHIPS:-

- A number of important equations and operating characteristics have been introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT transistor. The JFET equations are defined for the configuration of Fig. 13a, while the BJT equations relate to Fig. 13b.



(a) JFET versus (b) BJT.

Figure (13)

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

DEPLETION-TYPE MOSFET :-

- As noted in the chapter introduction, there are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation, while the label MOSFET stands for metal-oxide-semiconductor-field-effect transistor.
- Basic Construction:-
- The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 14. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 14.

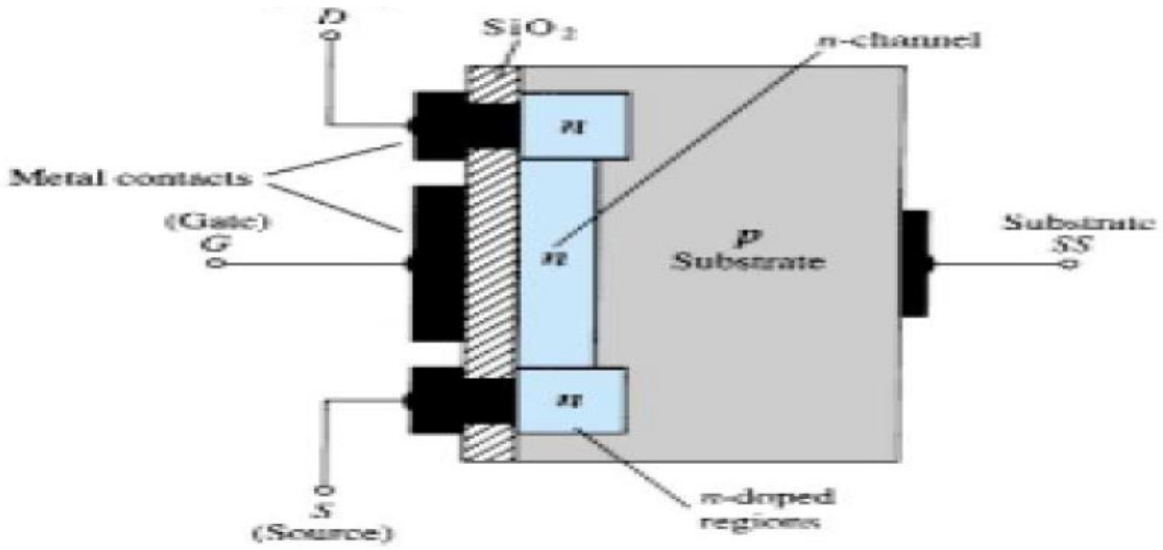
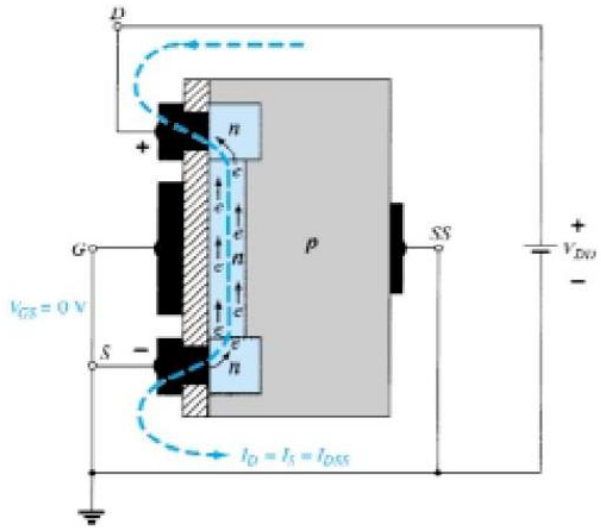


Figure (14) *n*-Channel depletion-type MOSFET.

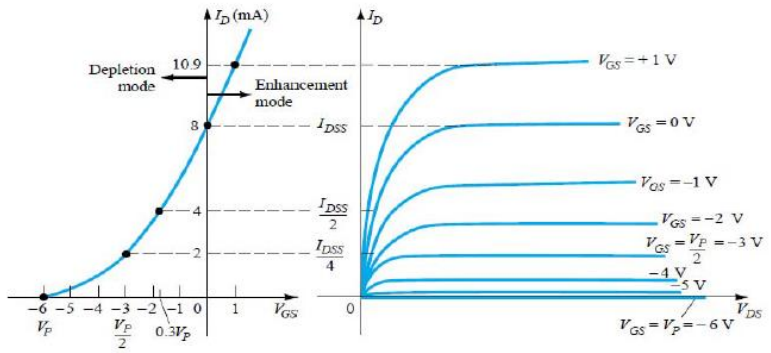
- The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO2) layer.
- The fact that the SiO2 layer is an insulating layer reveals the following
- fact: There is no direct electrical connection between the gate terminal and the channel of a MOSFET.
- In addition: It is the insulating layer of SiO2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.
- The reason for the label metal-oxide-semiconductor FET is now fairly obvious:

- *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated gate FET* or *IGFET.*
- Basic Operation and Characteristics
- In Fig. 15 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage *VDS* is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with *VGS* = 0 V continues to be labeled *IDSS*, as shown in Fig. 16.



n-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}.

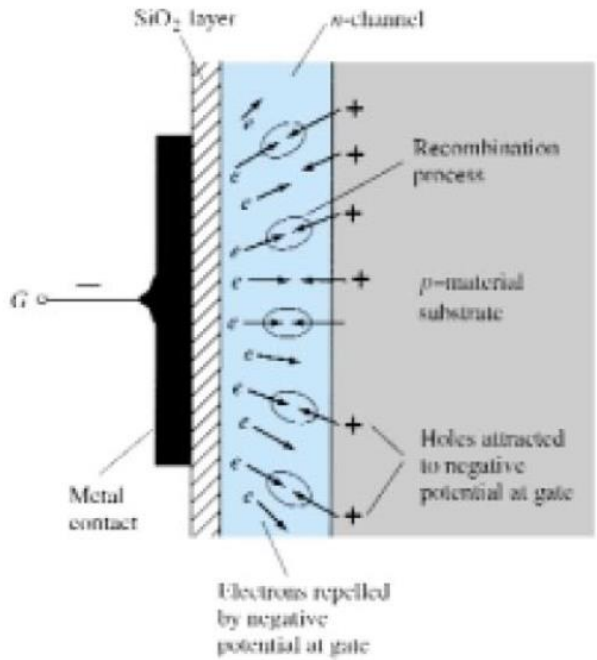
Figure (15)



Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

Figure (16)

- In Fig. 17, *VGS* has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 17. Depending on the magnitude of the negative bias established by *VGS*, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for *VGS* as shown in Fig. 16 for *VGS*=-1 V, -2 V, and so on, to the pinch-off level of -6 V.



Reduction in free carriers in channel due to a negative potential at the gate terminal.

Figure (17)

- For positive values of *VGS*, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 16 reveals that the drain current will increase at a rapid rate for the reasons listed above.
- That is, for the device of Fig. 16, the application of a voltage *VGS*=+4 V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has “enhanced” the level of free carriers in the channel compared to that encountered with *VGS* =0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of *IDSS* referred to as the *depletion region.*

EXAMPLE:

Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with *IDSS* = 10 mA and *VP* = - 4 V?

Solution

At $V_{GS} = 0$ V, $I_D = I_{DSS} = 10$ mA

$V_{GS} = V_P = -4$ V, $I_D = 0$ mA

$V_{GS} = \frac{V_P}{2} = \frac{-4\text{ V}}{2} = -2$ V, $I_D = \frac{I_{DSS}}{4} = \frac{10\text{ mA}}{4} = 2.5$ mA

and at $I_D = \frac{I_{DSS}}{2}$, $V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2$ V

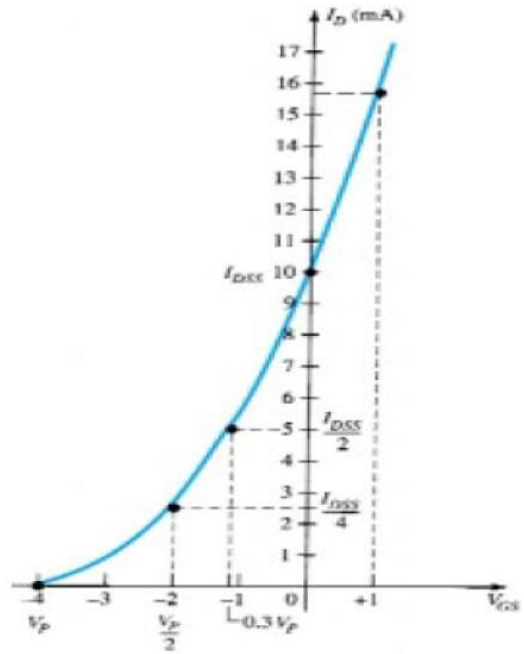

I_D (mA)
17
16
15
14
13
12
11
I_{DSS} 10
9
8
7
6
5
$\frac{I_{DSS}}{2}$
4
3
$\frac{I_{DSS}}{4}$
2
1
−4
−3
−2
−1
0
+1
V_{GS}
V_P
$\frac{V_P}{2}$
$0.3V_P$

Figure (18)

- Before plotting the positive region of *VGS*, keep in mind that *ID* increases very rapidly with increasing positive values of *VGS*. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we will try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

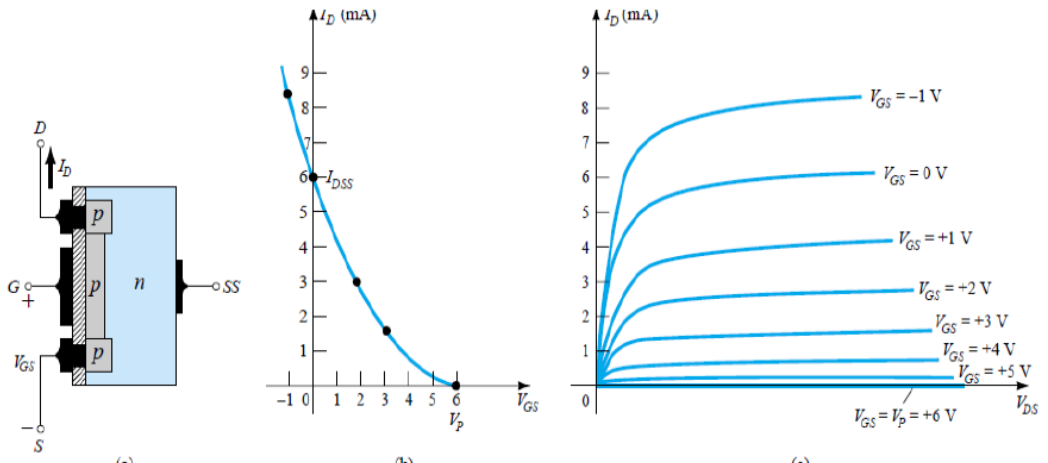
$$= 10\text{ mA}\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = 10\text{ mA}(1 + 0.25)^2 = 10\text{ mA}(1.5625)$$

$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.

p-Channel Depletion-Type MOSFET:-

- The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 14. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 19a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure.
- The drain characteristics would appear exactly as in Fig. 16 but with *VDS* having negative values, *ID* having positive values as indicated (since the defined direction is now reversed), and *VGS* having the opposite polarities as shown in Fig. 19c. The reversal in *VGS* will result in a mirror image (about the *ID* axis) for the transfer characteristics as shown in Fig. 19b.
- In other words, the drain current will increase from cutoff at $VGS = VP$ in the positive *VGS* region to *IDSS* and then continue to increase for increasingly negative values of *VGS*. Shockley's equation is still applicable and requires simply placing the correct sign for both *VGS* and *VP* in the equation.



p-Channel depletion-type MOSFET with I_{DSS} = 6 mA and V_P = +6 V.

Figure (19)

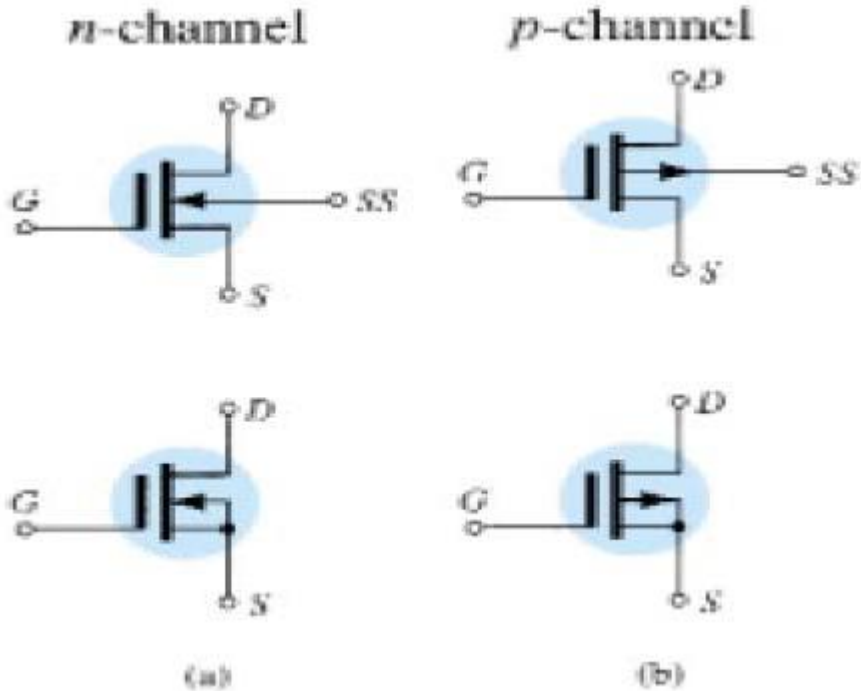
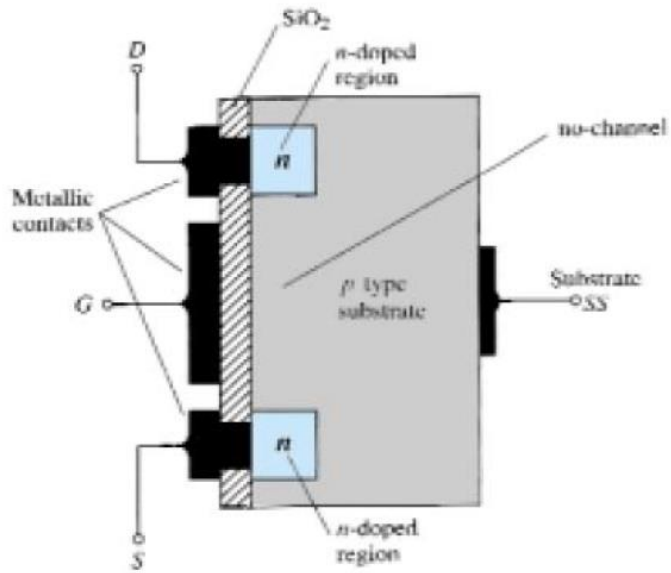


Figure (19) Graphic symbols for (a) *n*-channel depletion-type MOSFETs and (b) *p*-channel depletion-type MOSFETs.

ENHANCEMENT-TYPE MOSFET:-

- Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement type MOSFET are quite different from anything obtained thus far.
- The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 20. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.



n-Channel enhancement-type MOSFET.

Figure (20)

- The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 20 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device.
- The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

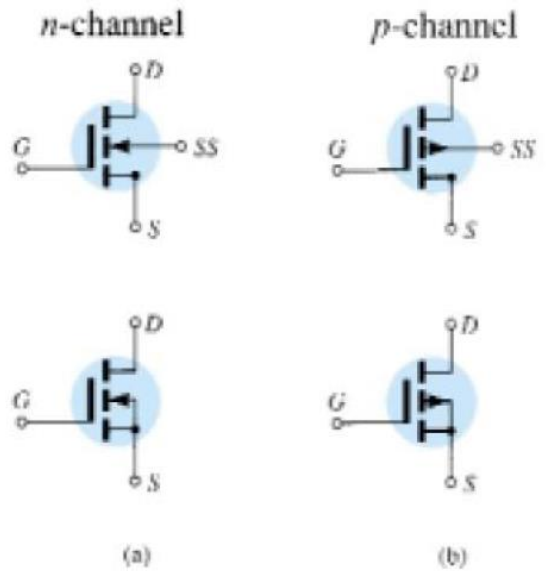
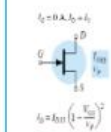
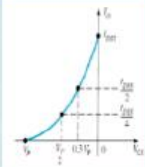
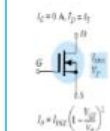
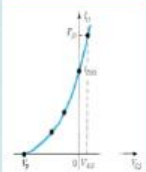
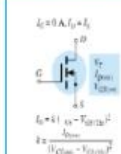
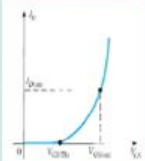


Figure (21)

Symbols for (a) *n*-channel enhancement-type MOSFETs and (b) *p*-channel enhancement-type MOSFETs.

Type	Symbol Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (*n*-channel)			$R_i > 100\ \text{M}\Omega$ C_i (1 – 10) pF
MOSFET depletion-type (*n*-channel)			$R_i > 10^{10}\ \Omega$ C_i (1 – 10) pF
MOSFET enhancement-type (*n*-channel)			$R_i > 10^{10}\ \Omega$ C_i (1 – 10) pF

FET BAISING:-

- The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A}$$

$$I_D = I_S$$

- For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

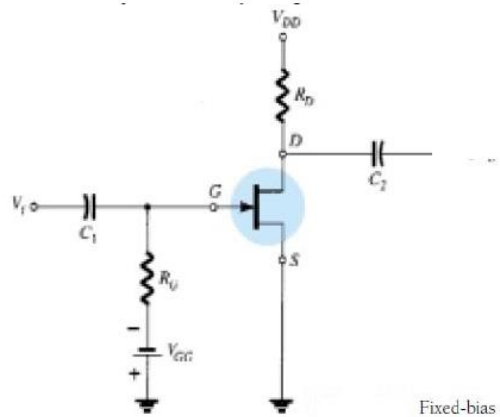
$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2$$

- For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2$$

FIXED-BIAS CONFIGURATION:

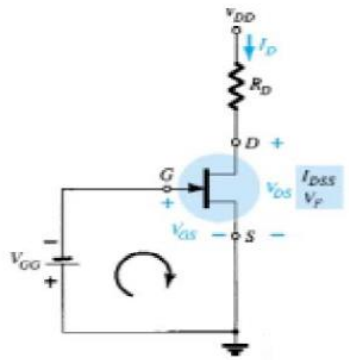
- The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. -22 - Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.



Fixed-bias configuration.

Figure (22)

- The configuration of Fig. 22 includes the ac levels *Vi* and *Vo* and the coupling capacitors (*C*1 and *C*2). Recall that the coupling capacitors are “open circuits” for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor *RG* is present to ensure that *Vi* appears at the input to the FET amplifier for the ac analysis . For the dc analysis,
- The zero-volt drop across *RG* permits replacing *RG* by a short-circuit equivalent, as appearing in the network of Fig. 23 specifically redrawn for the dc analysis.



Network for dc analysis.

Figure (23)

- Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 6.2 will result in

$$-V_{GG} - V_{GS} = 0$$

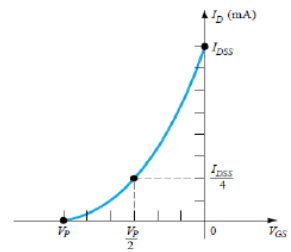
$$\boxed{V_{GS} = -V_{GG}}$$

- Since *VGG* is a fixed dc supply, the voltage *VGS* is fixed in magnitude, resulting in the notation "fixed-bias configuration."

- The resulting level of drain current *ID* is now controlled by Shockley's equation:

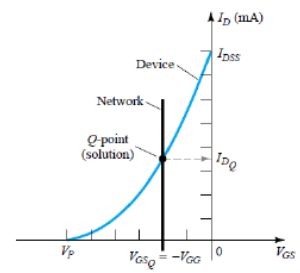
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- A graphical analysis would require a plot of Shockley's equation as shown in Fig. 6.3. Recall that choosing *VGS*_ *VP*/2 will result in a drain current of *IDSS*/4 when plotting the equation. For the analysis of this chapter, the three points defined by *IDSS*, *VP*, and the intersection just described will be sufficient for plotting the curve.



Plotting Shockley's equation.

- In Fig. 6.4, the fixed level of *VGS* has been superimposed as a vertical line at *VGS* = -*VGG*. At any point on the vertical line, the level of *VGS* is -*VGG*—the level of *ID* must simply be determined on this vertical line.



Finding the solution for the fixed-bias configuration.

Figure (24)

- The point where the two curves intersect is the common solution to the configuration commonly referred to as the *quiescent* or *operating point.* The subscript *Q* will be applied to drain current and gate-to-source voltage to identify their levels at the *Q*-point. Note in Fig. 24 that the quiescent level of *ID* is determined by drawing a horizontal line from the *Q*-point to the vertical *ID* axis as shown in Fig. 24.
- The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and $$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 6.2,

$$\boxed{V_S = 0\ \text{V}}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

or $$V_D = V_{DS} + V_S = V_{DS} + 0\ \text{V}$$

and $$\boxed{V_D = V_{DS}}$$

In addition, $$V_{GS} = V_G - V_S$$

or $$V_G = V_{GS} + V_S = V_{GS} + 0\ \text{V}$$

and $$\boxed{V_G = V_{GS}}$$

EXAMPLE:-

Determine the following for the network of Fig. 6.6.?

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.

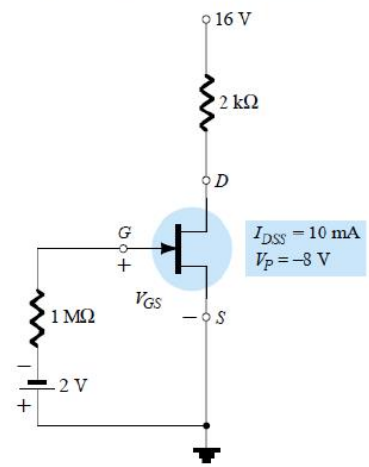


Figure (25)

Solution

Mathematical Approach:

(a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$

(b) $$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{-2\ \text{V}}{-8\ \text{V}}\right)^2$$
$$= 10\ \text{mA}(1 - 0.25)^2 = 10\ \text{mA}(0.75)^2 = 10\ \text{mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

(c) $$V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.625\ \text{mA})(2\ \text{k}\Omega)$$
$$= 16\ \text{V} - 11.25\ \text{V} = \mathbf{4.75\ V}$$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

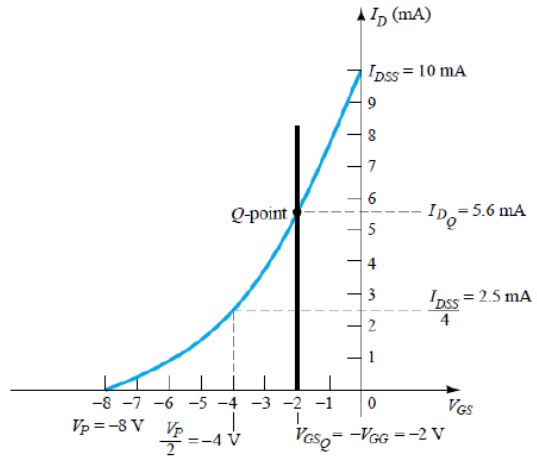
(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Graphical Approach:

The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig.

It is certainly difficult to read beyond the second place without significantly in-



Graphical solution for the network of Fig. 6.6.

Figure (26)

creasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 6.7 is quite acceptable. Therefore, for part (a),

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.