Mosfet

1- *Introduction*

The **Field Effect Transistor**, or simply **FET** however, use the voltage that is applied to their input terminal to control the output current, since their operation relies on the electric field (hence the name field effect) generated by the input voltage. This then makes the **Field Effect Transistor** a **VOLTAGE** operated device.

The **Field Effect Transistor** is a unipolar device that has very similar properties to those of the *Bipolar Transistor* ie, high efficiency, instant operation, robust and cheap, and they can be used in most circuit applications that use the equivalent Bipolar Junction Transistors, (BJT). They can be made much smaller than an equivalent BJT transistor and along with their low power consumption and dissipation make them ideal for use in integrated circuits such as the CMOS range of chips.

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We remember from the previous tutorials that there are two basic types of Bipolar Transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. There are also two basic types of Field Effect Transistor, N-channel and P-channel. As their name implies, Bipolar Transistors are "Bipolar" devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a "Unipolar" device that depends only on the conduction of Electrons (N-channel) or Holes (P-channel).

2-The Junction Field Effect Transistor (JFET)

We saw previously that a bipolar junction transistor is constructed using two PN junctions in the main current path between the Emitter and the Collector terminals. The Field Effect Transistor has no junctions but instead has a narrow "Channel" of N-type or P-type silicon with electrical connections at either end commonly called the DRAIN and the SOURCE respectively. Both P-channel and N-channel FET's are available. Within this channel there is a third connection which is called the GATE and this can also be a P or N-type material forming a PN junction and these connections are compared below.

Bipolar Transistor	Field Effect Transistor
Emitter (E)	Source (S)
Base (B)	Gate (G)
Collector (C)	Drain (D)

The semiconductor "Channel" of the Junction Field Effect Transistor is a resistive path through which a voltage V_{ds} causes a current I_d to flow. A voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the drain terminal to the source terminal. The PN junction therefore has a high reverse bias at the drain terminal and a lower reverse bias at the source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias. FET's control the current flow through them between the drain and source terminals by controlling the voltage applied to the gate terminal. In an N-channel JFET this gate voltage is negative while for a P-channel JFET the gate voltage is positive.

2-1 Bias arrangements for a N-channel JFET and corresponding circuit symbols

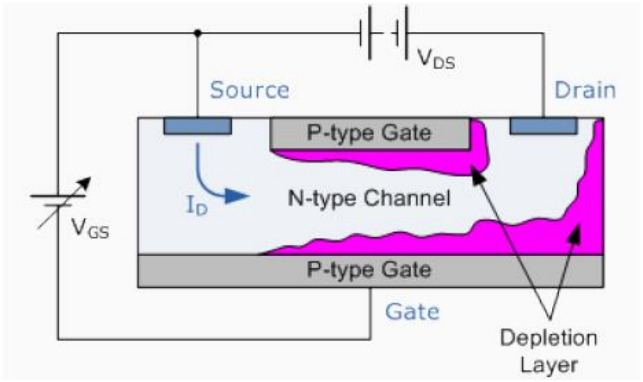

Figure (1)

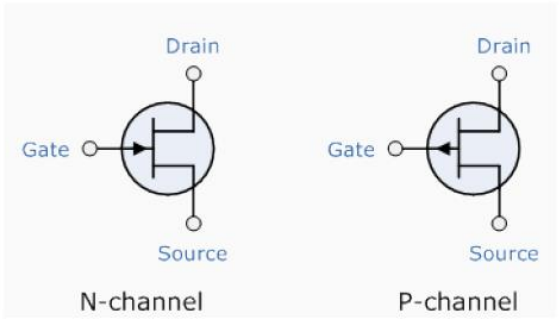

Figure (2)

The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the gate diffused into the N-type channel forming a reverse biased PN junction and its this junction which forms the **depletion layer** around the gate area. This depletion layer restricts the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel.

When the gate voltage V_g is equal to 0V and a small external voltage (V_{ds}) is applied between the drain and the source maximum current (I_d) will flow through the channel slightly restricted by the small depletion layer. If a negative voltage (V_{gs}) is now applied to the gate the size of the depletion layer begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect. As the gate voltage (V_{gs}) is made more negative, the width of the channel decreases until no more current flows between the drain and the source and the FET is said to be "**pinched-off**". In this pinch-off region the gate voltage, V_{gs} controls the channel current and V_{ds} has little or no effect. The result is that the FET acts more like a voltage controlled resistor which has zero resistance when V_{gs} = 0 and maximum "ON" resistance (R_{ds}) when the gate voltage is very negative.

2-2 Output characteristic voltage-current curves of a typical junction FET.

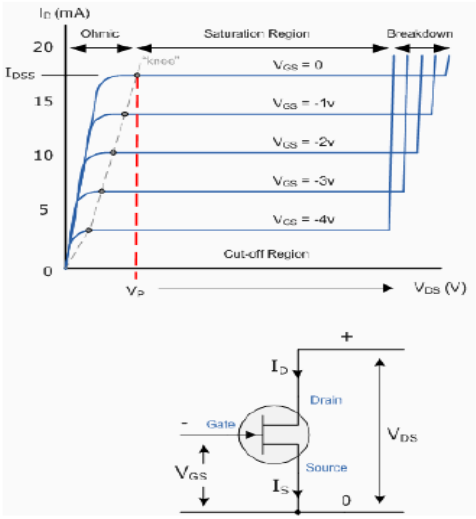

Figure (3)

- The voltage V_{gs} applied to the gate controls the current flowing between the drain and the source terminals. V_{gs} refers to the voltage applied between the gate and the source while V_{ds} refers to the voltage applied between the drain and the source. Because a **Field Effect Transistor** is a VOLTAGE controlled device, "NO current flows into the gate!" then the source current (I_s) flowing out of the device equals the drain current flowing into it and therefore ($I_d = I_s$).
- The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

• Ohmic Region - The depletion layer of the channel is very small and the JFET acts like a variable resistor.

• Cut-off Region - The gate voltage is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

• Saturation or Active Region - The JFET becomes a good conductor and is controlled by the gate-source voltage, (V_{gs}) while the drain-source voltage, (V_{ds}) has little or no effect.

- Breakdown Region - The voltage between the drain and source, (V_{ds}) is high enough to causes the JFET's resistive channel to break down and pass current.
- The control of the drain current by a negative gate potential makes the **Junction Field Effect Transistor** useful as a switch and it is essential that the gate voltage is never positive for an N-channel JFET as the channel current will flow to the gate and not the drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed

3- The MOSFET

- As well as the Junction Field Effect Transistor, there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor**. The most common type of insulated gate FET or IGFET as it is sometimes called, is the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.
- The **MOSFET** type of field effect transistor has a "Metal Oxide" gate (usually silicon dioxide commonly known as glass), which is electrically insulated from the main semiconductor N-channel or P-channel. This isolation of the controlling gate makes the input resistance of the **MOSFET** extremely high in the Mega-ohms region and almost infinite. As the gate terminal is isolated from the main current carrying channel ""NO current flows into the gate"" and like the JFET, the **MOSFET** also acts like a voltage controlled resistor. Also like the JFET, this very high input resistance can easily accumulate large static charges resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

3-1 Basic MOSFET Structure and Symbol

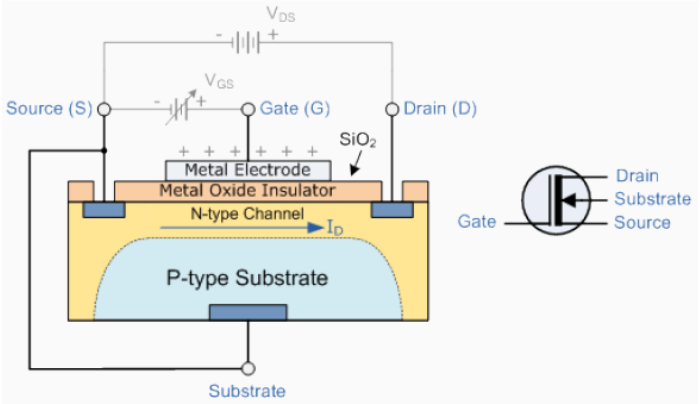

Figure (4)

- We also saw previously that the gate of a JFET must be biased in such a way as to forward-bias the PN junction but in a MOSFET device no such limitations applies so it is possible to bias the gate in either polarity. This makes MOSFET's specially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and the high gate resistance means that very little control current is needed. Both the P-channel and the N-channel MOSFET is available in two basic forms, the **Enhancement** type and the **Depletion** type.

3-2 Depletion-mode MOSFET

The **Depletion-mode MOSFET**, which is less common than the enhancement types is normally switched "ON" without a gate bias voltage but requires a gate to source voltage (V_{gs}) to switch the device "OFF". Similar to the JFET types. For N-channel MOSFET's a "Positive" gate voltage widens the channel, increasing the flow of the drain current and decreasing the drain current as the gate voltage goes more negative. The opposite is also true for the P-channel types. The depletion mode MOSFET is equivalent to a "Normally Closed" switch.

3-2-1 Depletion-mode N-Channel MOSFET and circuit Symbols

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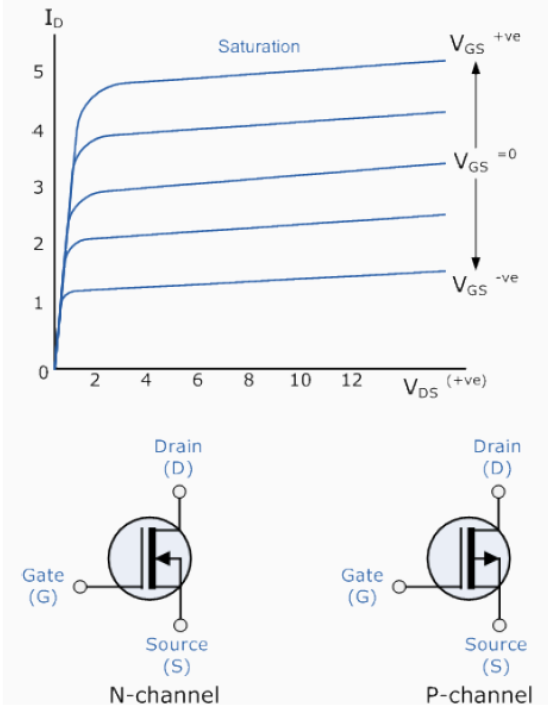
I_D
Saturation
V_{GS} +ve
V_{GS} =0
V_{GS} -ve
5
4
3
2
1
0
2
4
6
8
10
12
V_{DS} (+ve)
Drain (D)
Gate (G)
Source (S)
N-channel
Drain (D)
Gate (G)
Source (S)
P-channel

Figure (5)

Depletion-mode MOSFET's are constructed similar to their JFET transistor counterparts where the drain-source channel is inherently conductive with electrons and holes already present within the N-type or P-type channel. This doping of the channel produces a conducting path of low resistance between the drain and source with zero gate bias.

3-3 Enhancement-mode MOSFET

- The more common **Enhancement-mode MOSFET** is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally "OFF" when the gate bias voltage is equal to zero.
- A drain current will only flow when a gate voltage (V_{gs}) is applied to the gate terminal. This positive voltage creates an electrical field within the channel attracting electrons towards the oxide layer and thereby reducing the overall resistance of the channel allowing current to flow. Increasing this positive gate voltage will cause an increase in the drain current, I_d through the channel. Then, the Enhancement-mode device is equivalent to a "Normally Open" switch.

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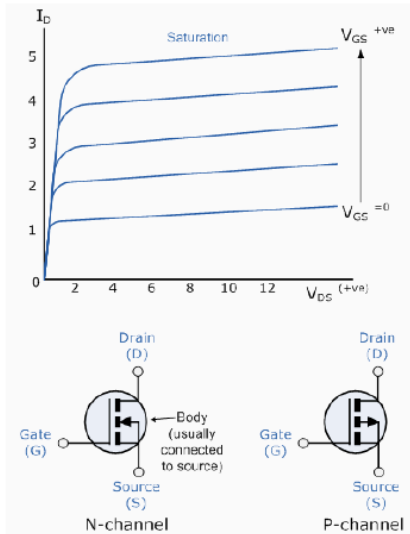
I_D
Saturation
V_{GS} +ve
5
4
3
2
1
0
2 4 6 8 10 12
V_{DS} (+ve)
V_{GS} =0
Drain (D)
Gate (G)
Body (usually connected to source)
Source (S)
N-channel
Drain (D)
Gate (G)
Source (S)
P-channel

Figure (6)

Enhancement-mode MOSFET's make excellent electronics switches due to their low "ON" resistance and extremely high "OFF" resistance and extremely high gate resistance. Enhancement-mode MOSFET's are used in integrated circuits to produce CMOS type **Logic Gates** and power switching circuits as they can be driven by digital logic.

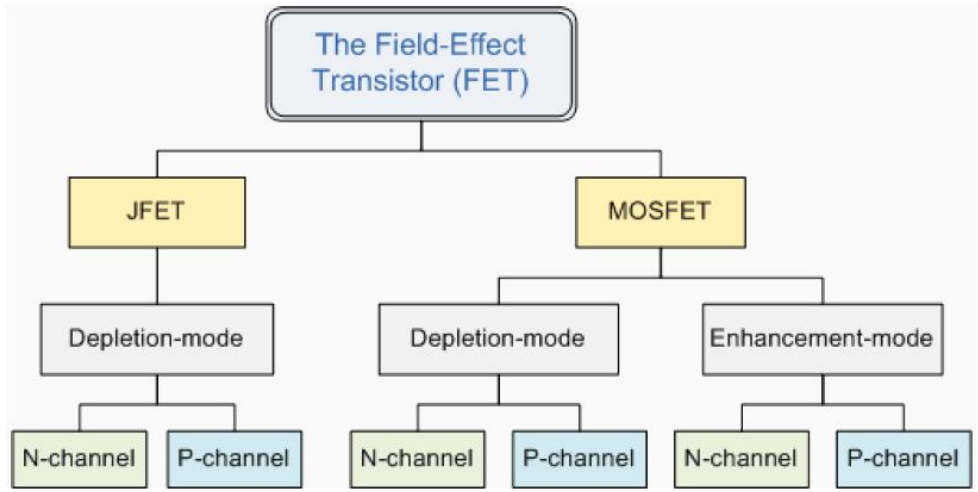
The Field-Effect Transistor (FET)
JFET
MOSFET
Depletion-mode
Depletion-mode
Enhancement-mode
N-channel
P-channel
N-channel
P-channel
N-channel
P-channel

Figure (7)