University Of Diyala
College Of Engineering
Computer Engineering Department

COMPUTER ARCHITECTURE II

PART 5: MULTIPROCESSORS AND THREAD-LEVEL PARALLELISM

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Second stage

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Thread-Level Parallelism

- **Parallel processing :** a term used to denote a large class of techniques that are used to provide simultaneous data processing tasks for the purpose of increasing the computational speed of a computer system.
- **Pipelining :** a technique of decomposing a sequential process into sub operations, with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.
- **Thread** : process with its own instructions and data.
- **Thread-Level Parallelism :** execution of multiple program concurrently.

Multi-core processors **Multiprocessors**

Multi-core processors

- **Limitation in the clock frequency of single core.**
- **The new programs and applications are multithreaded.**
- **The need for parallel processing.**

Processor	Series	Cores	L3 cache	Power (typical)	Clock rate (GHz)	Price
Xeon	7500	8	18–24 MB	130 W	2–2.3	$2837–3692
Xeon	5600	4–6 w/wo SMT	12 MB	40–130 W	1.86–3.33	$440–1663
Xeon	3400–3500	4 w/wo SMT	8 MB	45–130 W	1.86–3.3	$189–999
Xeon	5500	2–4	4–8 MB	80–130 W	1.86–3.3	$80–1600
i7	860–975	4	8 MB	82 W–130 W	2.53–3.33	$284–999
i7 mobile	720–970	4	6–8 MB	45–55 W	1.6–2.1	$364–378
i5	750–760	4 wo SMT	8 MB	80 W	2.4–2.8	$196–209
i3	330–350	2 w/wo SMT	3 MB	35 W	2.1–2.3	

Characteristics of Multiprocessors

- ***A multiprocessor system*** is an interconnection of two or more CPUs with memory and input-output equipment.

- The term "processor" in multiprocessor can mean either a central processing unit (CPU) or an input-output processor (IOP).

- Multiprocessors (also multi core processors) are classified as ***multiple instruction stream***, ***multiple data stream*** **(MIMD)** systems.

Multiprocessor system as parallel system

- **The system derives its high performance from the fact that computations can proceed in parallel in one of two ways:**

1. **Multiple independent jobs can be made to operate in parallel.**
2. **A single job can be partitioned into multiple parallel tasks.**

- **Improving performance by decomposing a program into parallel executable tasks. (two ways)**

1. **The user can explicitly declare that certain tasks of the program be executed in parallel. (done prior to loading the program) and (with help of OS).**
2. **(more efficient) way is to provide a compiler with multiprocessor software that can automatically detect parallelism in a user's program.**

- **What is the parallelizing compiler?**

Multiprocessors classification

Tightly coupled or Shared- Memory System

- Each processor can have its own local memory (cache memory)
- A global common memory (Shared memory) that all CPUs can access.
- Information shared among the CPUs by placing it in the common global memory.

Loosely Coupled or Distributed-Memory System

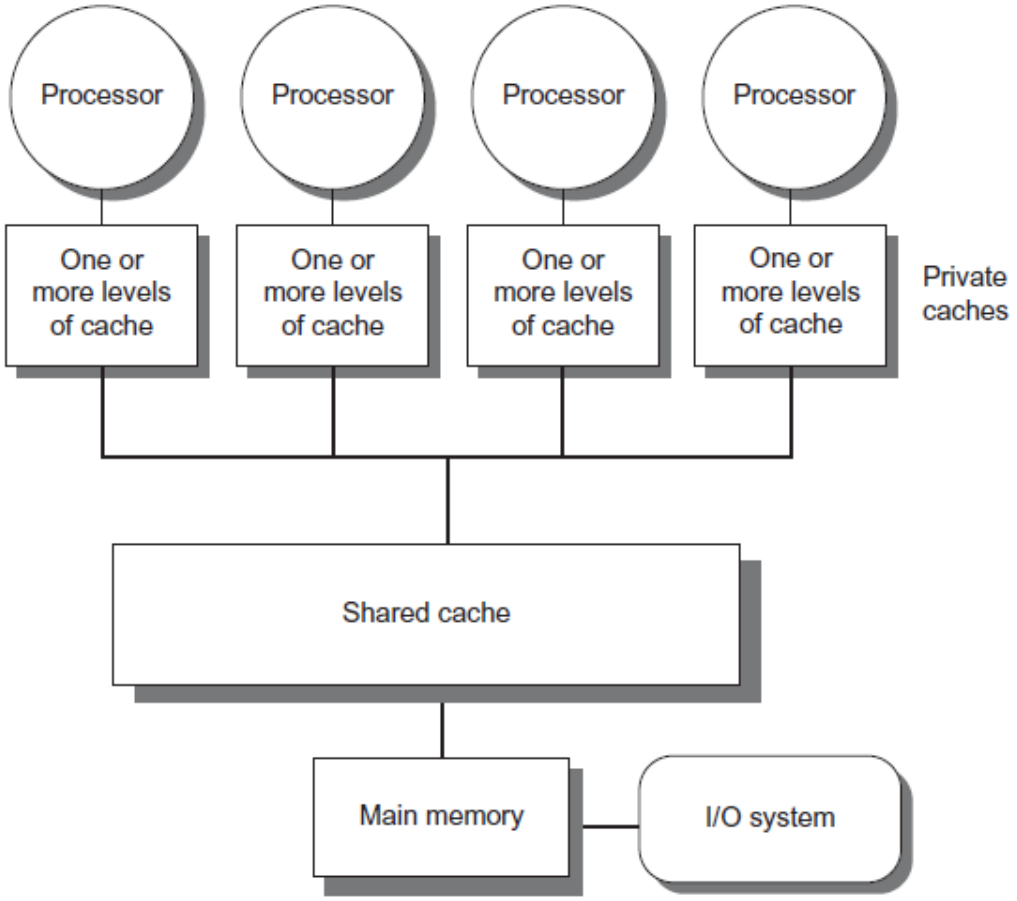
- Each processor element has its own private local memory.
- The processors are tied together by a switching scheme designed to route information from one processor to another through a message-passing scheme.
- The processors relay program and data to other processors in packets.

NOTES

- Loosely coupled systems are most efficient when the interaction between tasks is minimal.
- Tightly coupled systems can tolerate a higher degree of interaction between tasks.

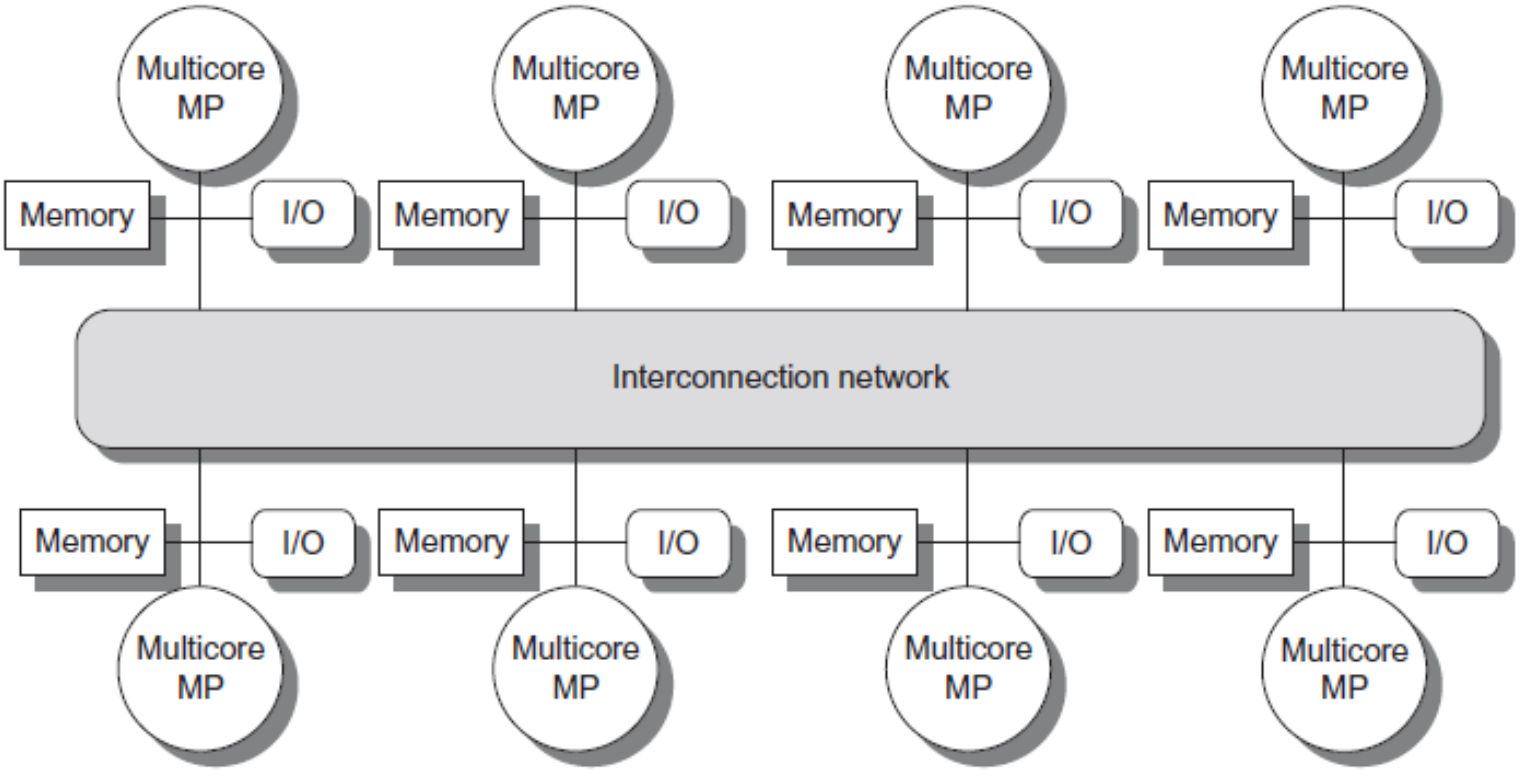
Multiprocessors classification

Tightly coupled or Shared- Memory System



Multiprocessors classification

Loosely Coupled: or Distributed-Memory System



Interconnection Structures

- **The components that form a multiprocessor system are:**

1. **CPUs,**
2. **IOPs connected to input-output devices**
3. **Memory unit that may be partitioned into a number of separate modules.**

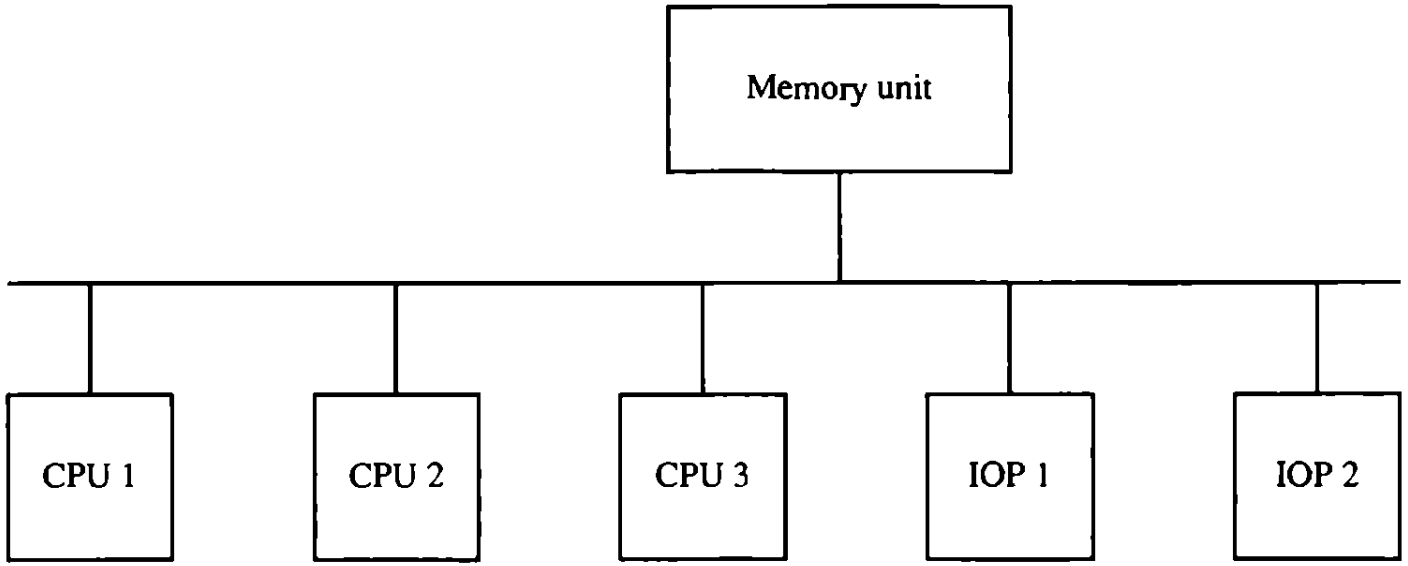
- **The interconnection between the components depending on:**
- The number of transfer paths that are available between the processors and memory in a **shared memory system**
- The number of transfer paths that are available among the processing elements in a **loosely coupled system.**

- **Some of interconnection forms:**

1. **Time-shared common bus**
2. **Multiport memory**
3. **Crossbar switch**
4. **Multistage switching network**
5. **Hypercube system**

Time Shared Common Bus-a single bus structure

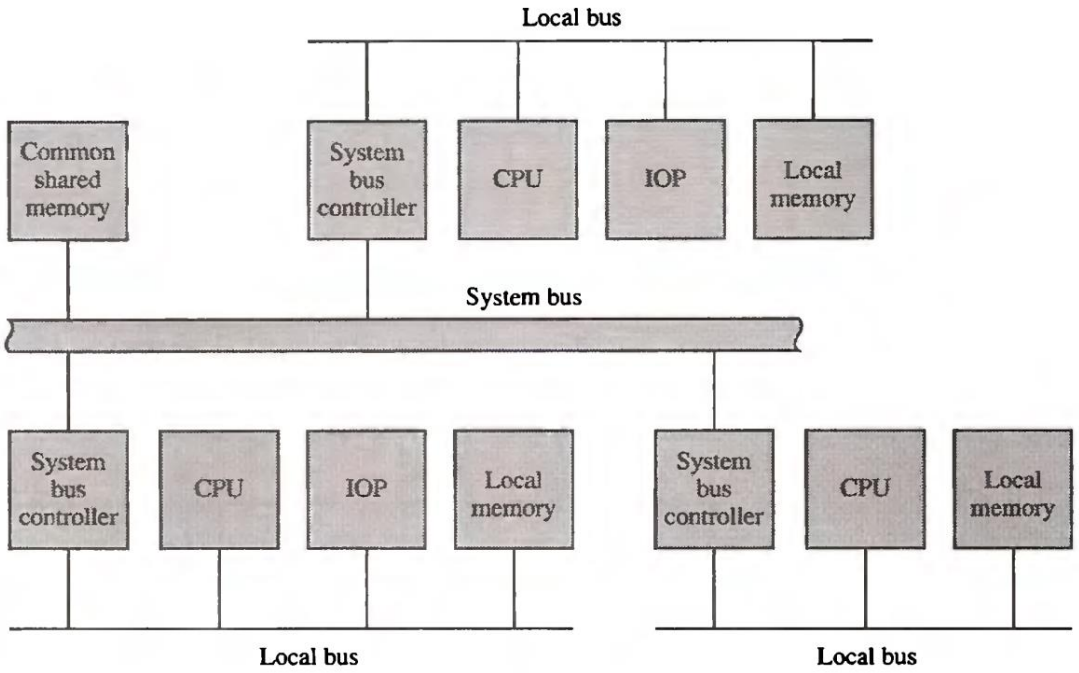
- **A number of processors connected through a common path to a memory unit.**



- **A single common-bus system is restricted to one transfer at a time.**
- **All other processors are either busy with internal operations or must be idle waiting for the bus.**
- **Conflicts must be resolved by incorporating a bus controller that establishes priorities among the requesting units.**

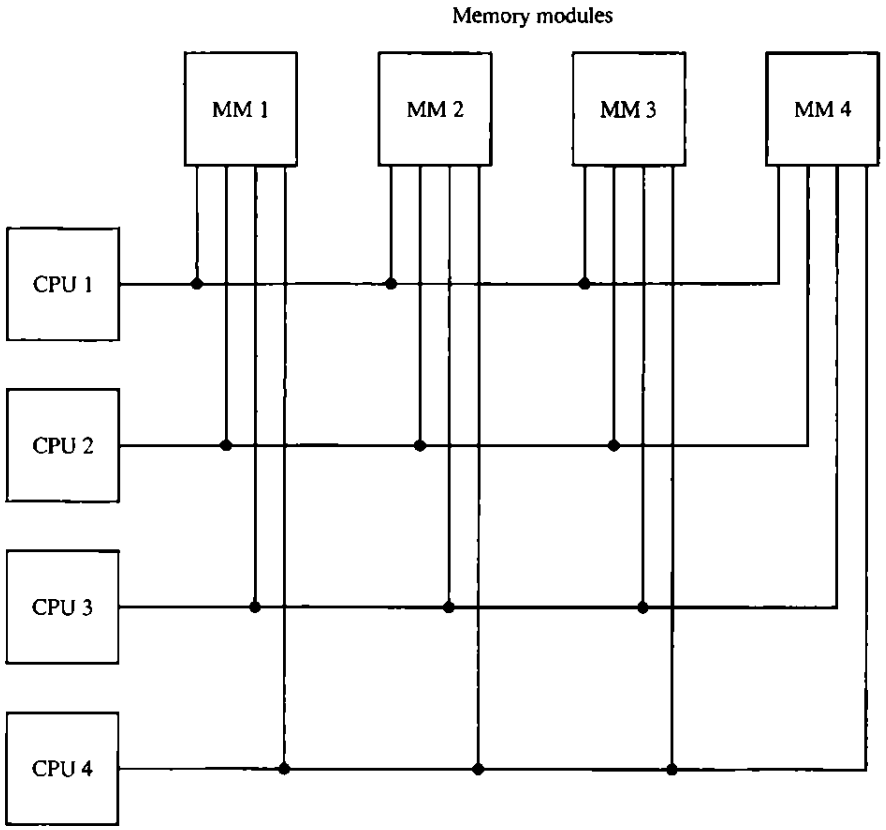
Time Shared Common Bus-a dual bus structure

- **Each local bus connected to its own local memory and to one or more processors.**
- **A system bus controller links each local bus to a common system bus.**
- **Only one processor can communicate with the shared memory and other common resources through the system bus at any given**



Multiport Memory

- **A multiport memory system employs separate buses between each memory module and each CPU.**
- **A processor bus consists of the address, data, and control lines required to communicate with memory.**



Multiport Memory

The advantage of the multiport memory organization

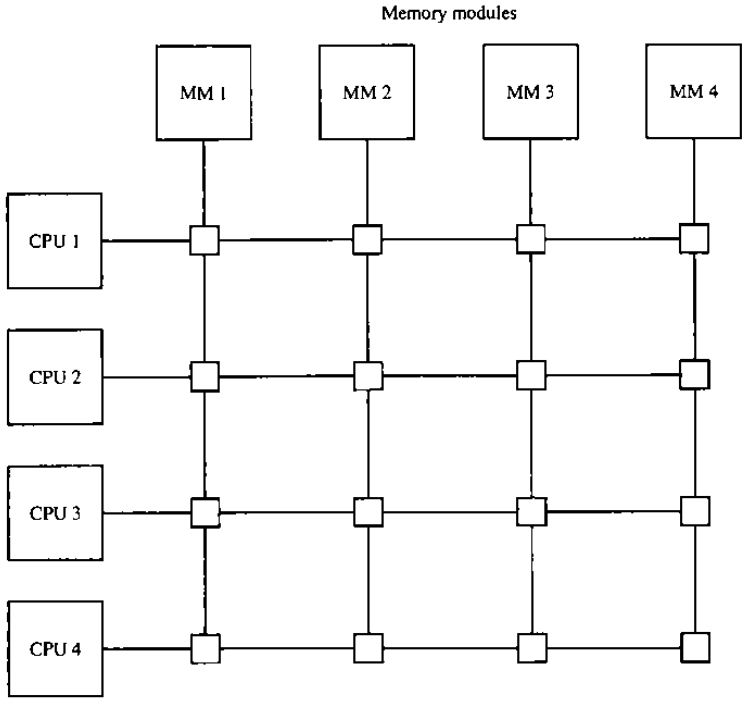
- **The high transfer rate that can be achieved because of the multiple paths between processors and memory.**

The disadvantage

- **It requires expensive memory control logic and a large number of cables and connectors. As a consequence, this interconnection structure is usually appropriate for systems with a small number of processors.**

Crossbar Switch

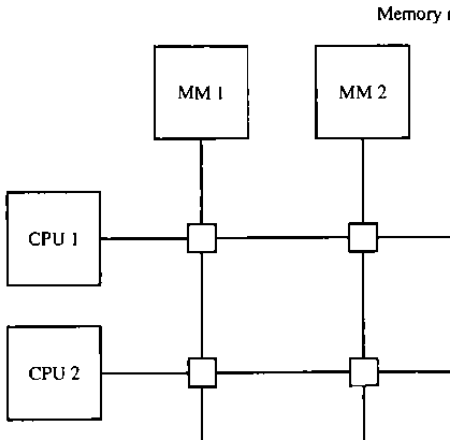
- **The crossbar switch organization consists of a number of cross points that are placed at intersections between processor buses and memory module paths.**
- **A switch that determines the path from a processor to a memory module.**
- **Each switch point has control logic to set up the transfer path between a processor and memory.**



Crossbar Switch

Crossbar switch-control logic

- **It examines the address that is placed in the bus to determine whether its particular module is being addressed.**
- **It resolves multiple requests for access to the same memory module on a predetermined priority basis.**
- **Priority levels are established by the arbitration logic to select one Crossbar switch input when two or more CPUs attempt to access the same memory.**



Crossbar Switch

Advantage

- **A crossbar switch organization supports simultaneous transfers from memory modules because there is a separate path associated with each module.**

Disadvantage

- **The hardware required to implement the switch can become quite large and complex.**