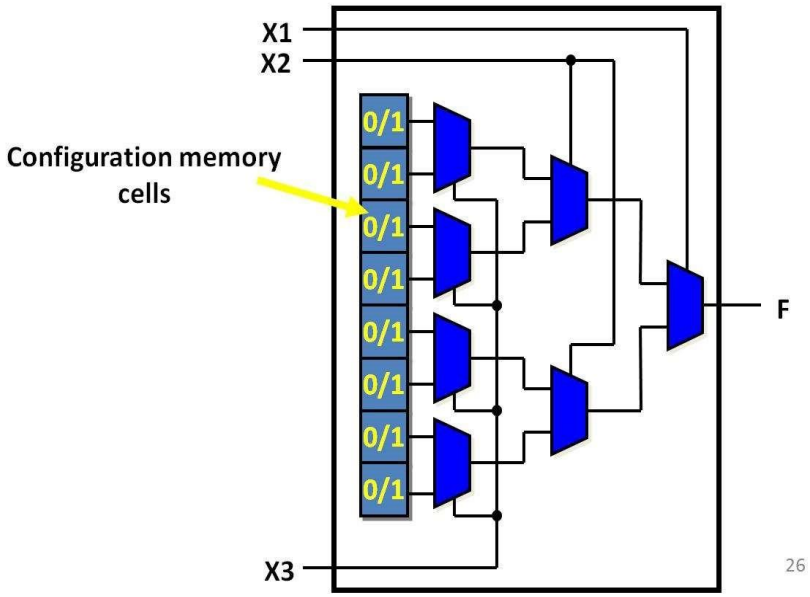
multiplexers Implementation



X3	X2	X1	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

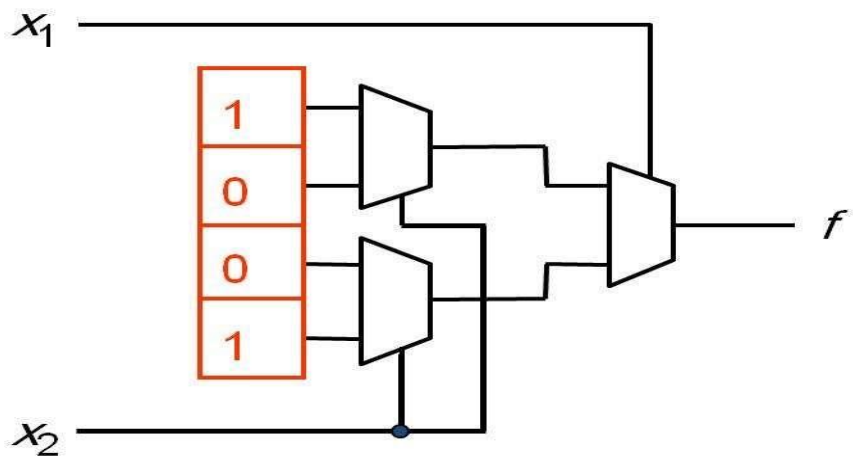
1. Put X3 at level 1
2. Put X2 at level 2
3. Put X1 at level 3 o\p

- Example 2 Input LUT

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	1

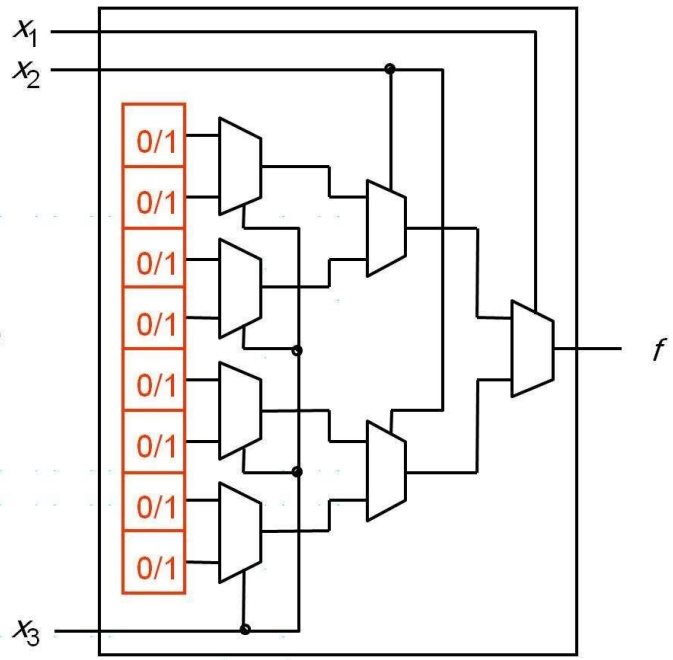
f = $x_1'x_2'$ + x_1x_2, or using Shannon's expansion:

f = $x_1'(x_2')$ + $x_1(x_2)$
= $x_1'(x_2'(1)$ + $x_2(0))$ + $x_1(x_2'(0)$ + $x_2(1))$



Implementation LUT with 3 input

- 3 Input LUT
  - 7 2x1 MUXes and 8 storage cells are required
  - Commercial LUTs have 4-5 inputs, and 16-32 storage cells



Q1: you are asked to program an FPGA, whose LUTs and inter-connection wires are shown in **Figure below.** The function to be implemented is f = f1 _ f2, where f1 = a + b and f2 = a + c. LUT 1 should implement f1. LUT 2 should implement f2 and LUT 3 should implement f1-f2. The horizontally and vertically placed interconnection wires are fabricated in different planes. In order to depict a connection between these wires at a cross-point, place a cross-mark (X). The inputs a; b; c and the output f have already been connected to the "input-output pads