University Of Diyala
College Of Engineering
Department of Computer Engineering

Digital System Design II
Memories Overview

Dr. Yasir Al-Zubaidi

Third stage

2021

Memories

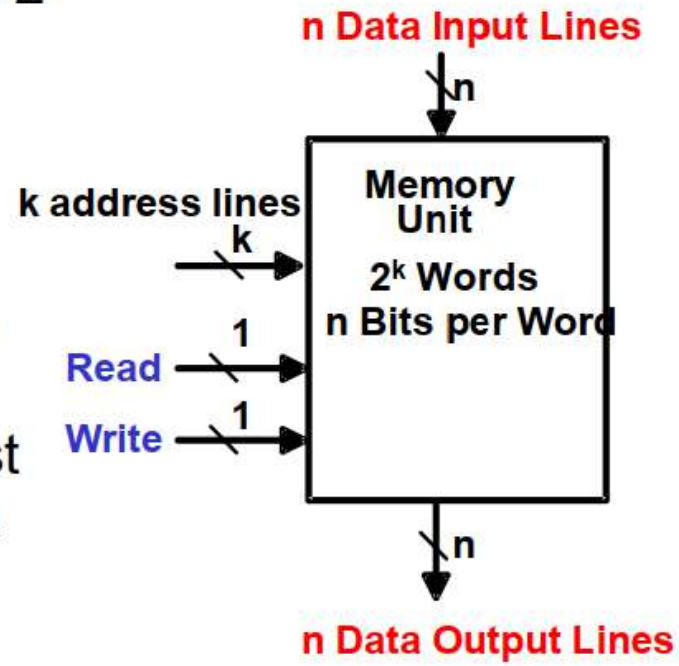
<table>
<tr><th colspan="3">Read-Write Memory</th><th>Read-Only Memory</th></tr>
<tr><td colspan="2">Volatile Memory</td><td>Non-volatile Memory</td><td rowspan="3">Mask-Programmed ROM (PROM) (nonvolatile)</td></tr>
<tr><td>Random Access</td><td>Sequential Access</td><td rowspan="2">EPROM
EEPROM
FLASH</td></tr>
<tr><td>DRAM
SRAM</td><td>FIFO
LIFO
Shift Register
CAM</td></tr>
</table>

- **Volatile: need electrical power**
- **Nonvolatile: magnetic disk, retains its stored information after the removal of power**
- **Random access: memory locations can be read or written in a random order**
- **EPROM: erasable programmable read-only memory**
- **EEPROM: electrically erasable programmable read-only memory**
- **FLASH: memory stick, USB disk**
- **Access pattern: sequential access: (video memory streaming) first-in-first-out (buffer), last-in-first-out (stack), shift register, content-addressable memory**

Memories

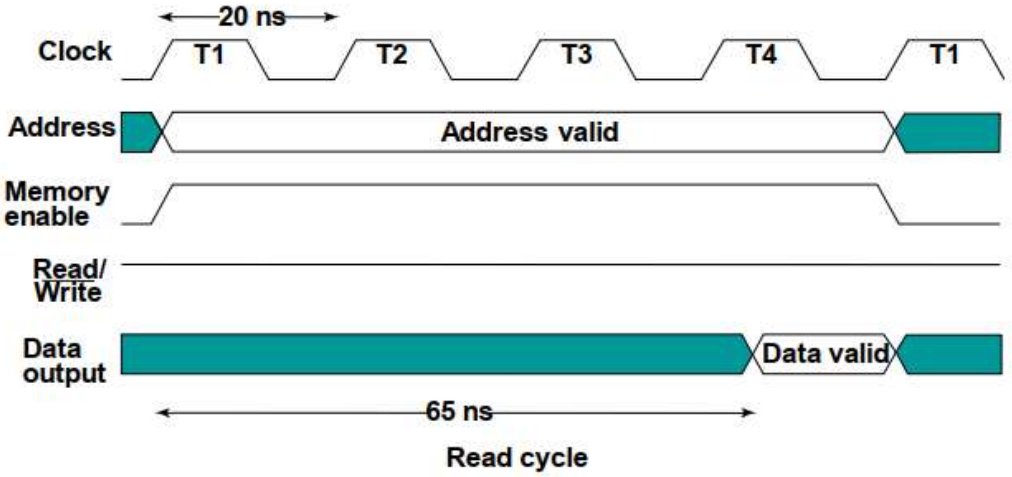
- k address lines are decoded to address 2^k words of memory.
- Each word is n bits.
- Read and Write are single control lines defining the simplest memory operations.

A basic memory system:



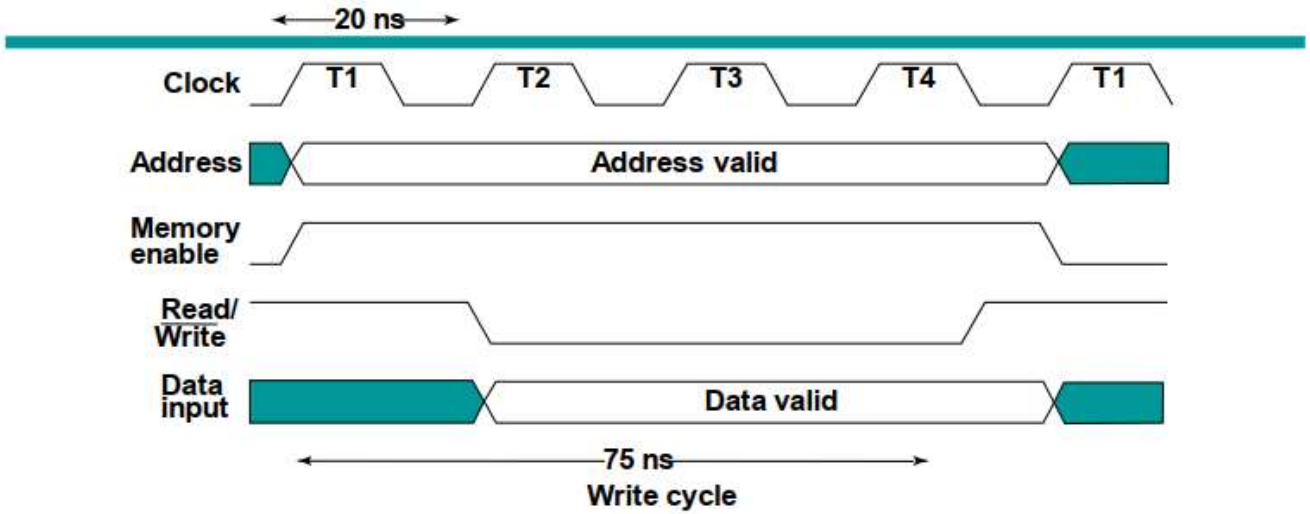
Memory Operation Timing - Reading

- Most basic memories are asynchronous
  - Storage in latches or storage of electrical charge
  - No clock
  - Controlled by control inputs and address, which are controlled by CPU and synchronized by its own clock
- Timing of signal changes/data observation is critical to the operation



- Read cycle: the access time, the maximum time from the application of the address to the appearance of the data at the Data output.

Memory Operation Timing - Writing



- Write cycle: the maximum time from the application of the address to the completion of all internal operations required to store a word
- Critical times measured with respect to edges of write pulse (1-0-1):
  - Address must be established at least a specified time before 1-0 and held for at least a specified time after 0-1 to avoid disturbing stored contents of other addresses
  - Data must be established at least a specified time before 0-1 and held for at least a specified time after 0-1 to write correctly

VHDL code for ROM

```
library IEEE;
use IEEE.std_logic_1164.all;

ENTITY rom8x4 IS
 PORT (
 addr: in std_logic_vector(2 downto 0);
 q: out std_logic_vector(3 downto 0));
END rom8x4;
```

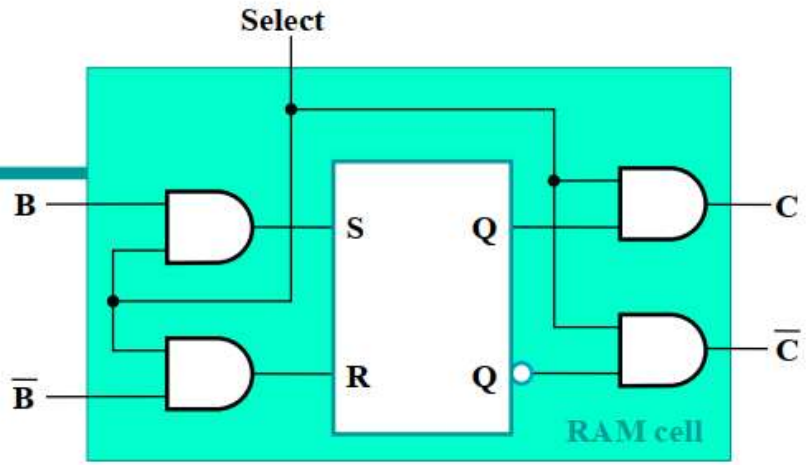
```
ARCHITECTURE behav OF rom8x4 IS
BEGIN

PROCESS(addr)
BEGIN
  CASE addr IS
    when "000" => q <= "0001";
    when "001" => q <= "0000";
    when "010" => q <= "0111";
    when "011" => q <= "1101";
    when "100" => q <= "1000";
    when "101" => q <= "1100";
    when "110" => q <= "0110";
    when "111" => q <= "1011";
    when others  =>  NULL;
  END case;
 END process;
END behav;
```

Random Access Memories (RAMs)

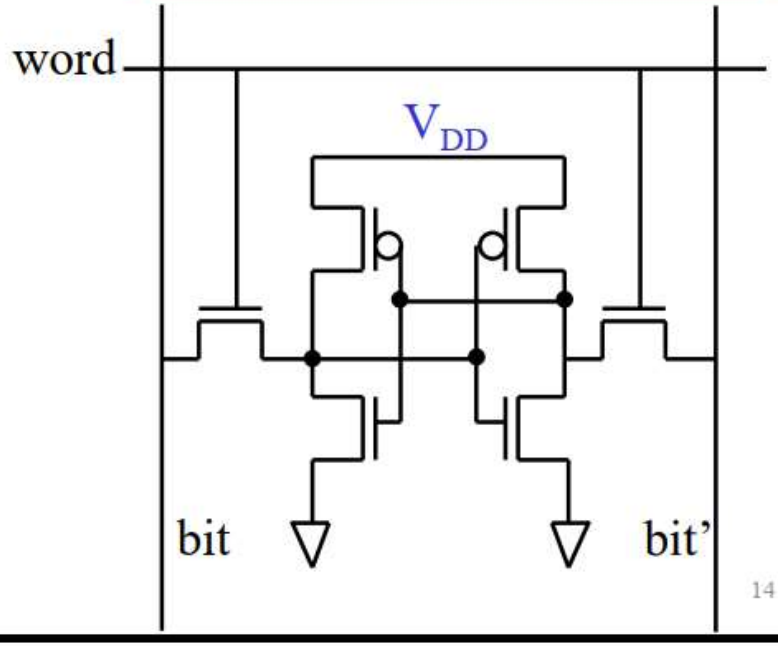
- Read/Write memory
- Types:
  - Static RAM (SRAM):
    - Once a word is written at a location, it remains stored as long as power is applied to the chip, unless the same location is written again.
    - Fast speed, but their cost per bit higher.
    - Application: Caches memories in Microprocessor
  - Dynamic RAM (DRAM):
    - The data stored at each location must be periodically refreshed by reading it and then writing it back again, otherwise it disappears.
    - Their density is greater and their cost per bit lower, but the speed is slower.

SRAM Cell

- Array of storage cells used to implement static RAM

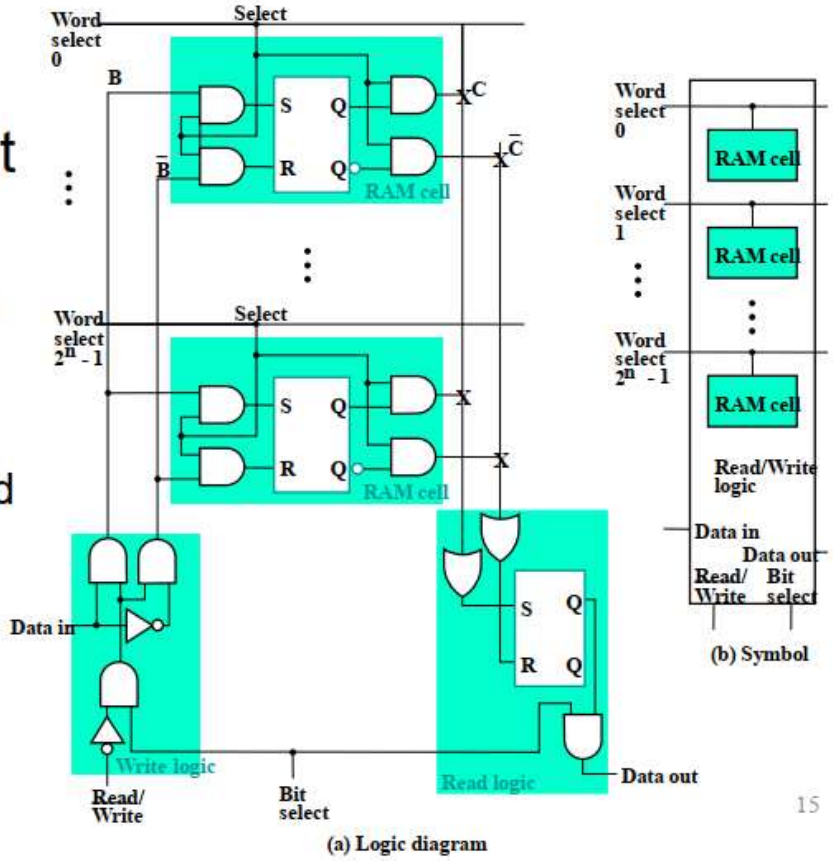


- Storage Cell
  - SR Latch
  - Input "Select" for control
  - Dual Rail Data
    - Inputs B and $\overline{B}$
    - Outputs C and $\overline{C}$



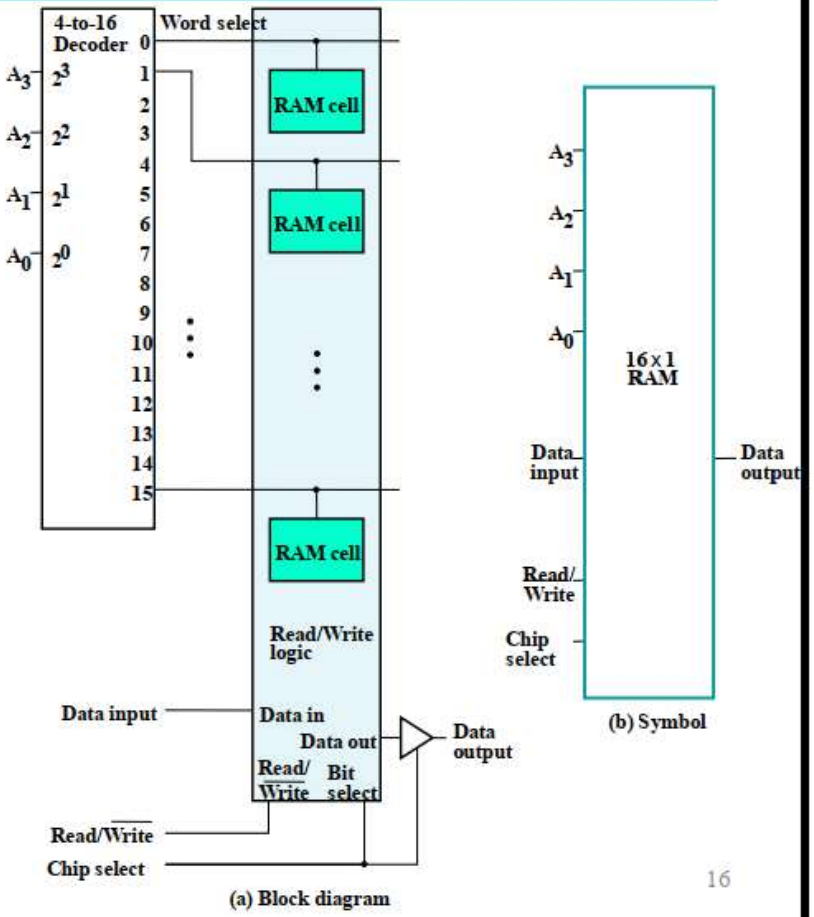
SRAM Bit Slice

- Represents all circuitry that is required for 2^n 1-bit words
  - Multiple RAM cells
  - Control Lines:
    - Word select i – one for each word
    - Read/$\overline{\text{Write}}$
    - Bit Select
  - Data Lines:
    - Data in
    - Data out



2^n-Word by 1-Bit RAM IC

- To build a RAM IC from a RAM slice:
  - Decoder decodes the n address lines to 2^n word select lines
  - A 3-state buffer on the data output permits RAM ICs to be combined into a RAM with $c \times 2^n$ words



Cell Arrays and Coincident Selection

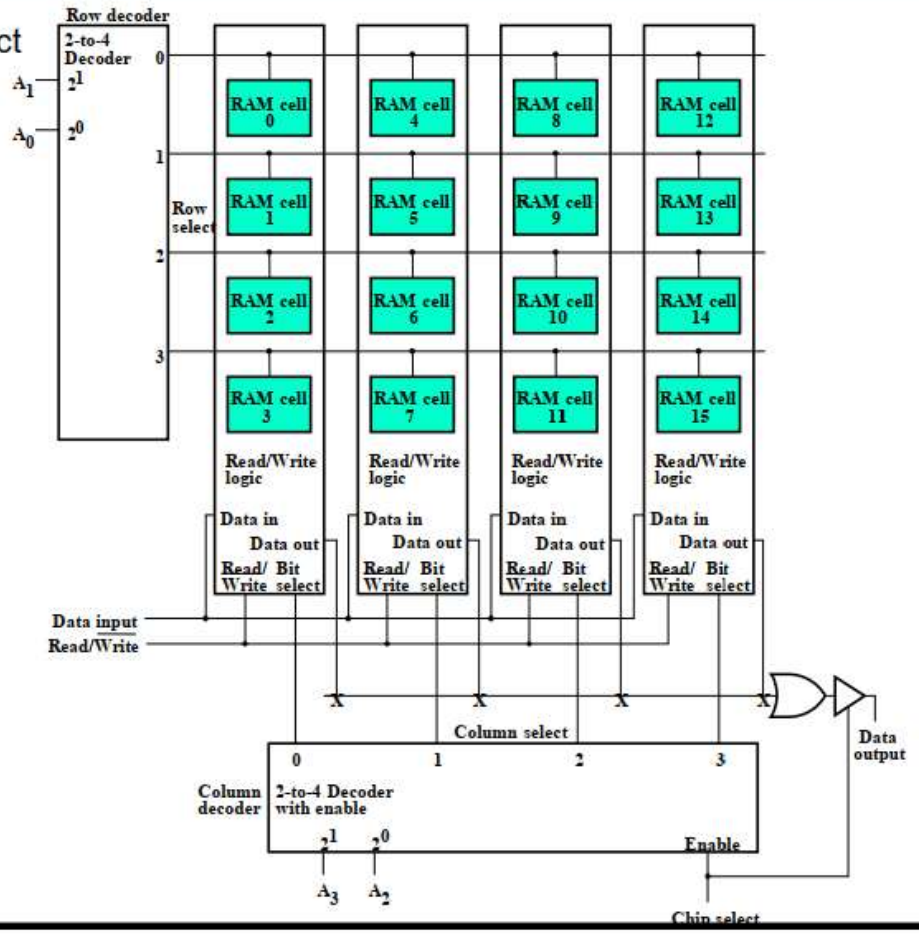
- Memory arrays can be very large =>
  - Large decoders
  - Large fanouts for the input bit lines
  - The decoder size and fanouts can be reduced by approximately $\sqrt{\mathbf{n}}$ using a coincident selection in a 2-D array: uses two decoders, one for words and one for bits:
    - Word select becomes Row select
    - Bit select becomes Column select

- See next slide for example

Cell Arrays and Coincident Selection (Contd.)

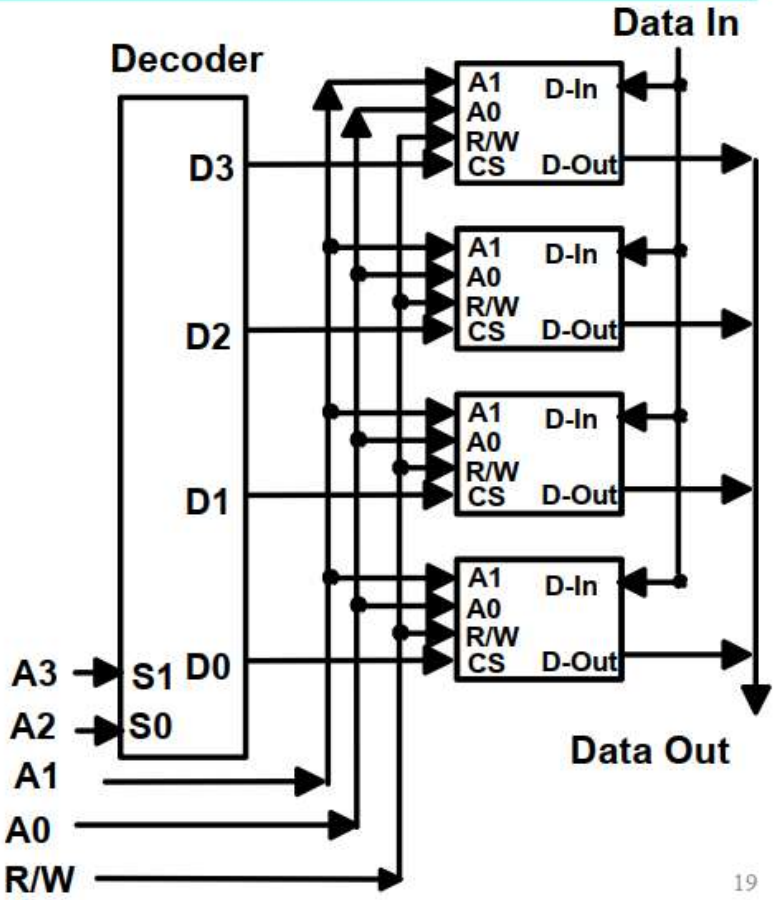
A_1 and A_0 used for Row select

A_3 and A_2 for Column select



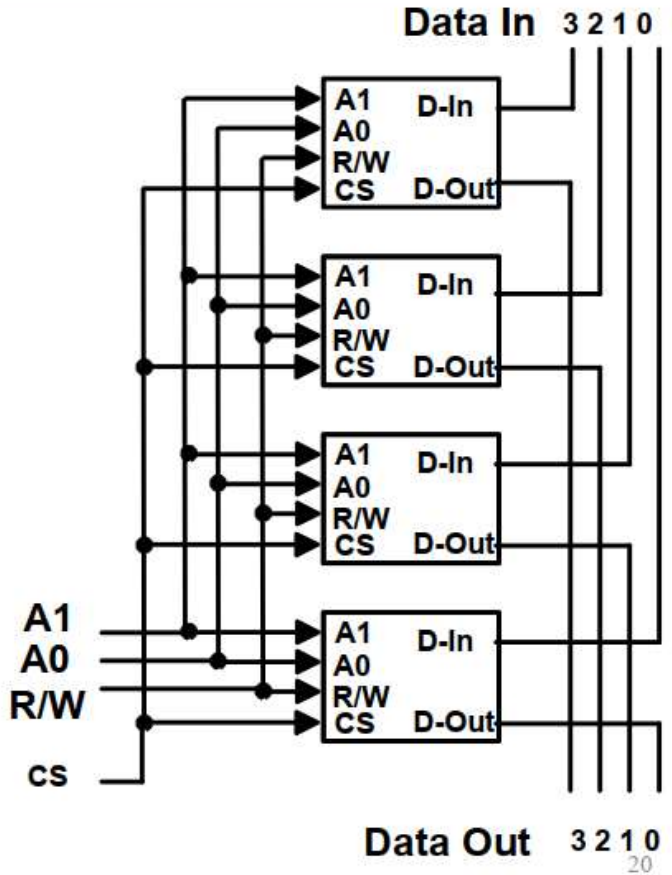
Making Larger Memories

- We can make larger memories from smaller ones by using the decoded higher order address bits to control CS (chip select) lines, tying all address, data, and R/W lines in parallel.
- A 16-Word by1-Bit memory constructed using 4-Word by 1-Bit memory.



Making Wider Memories

- Tie the address and control lines in parallel and keep the data lines separate.
- Example: make a 4-word by 4-bit memory from 4, 4-word by 1-bit memories
- Note: Both 16x1 and 4x4 memories take 4-chips and hold 16 bits of data.

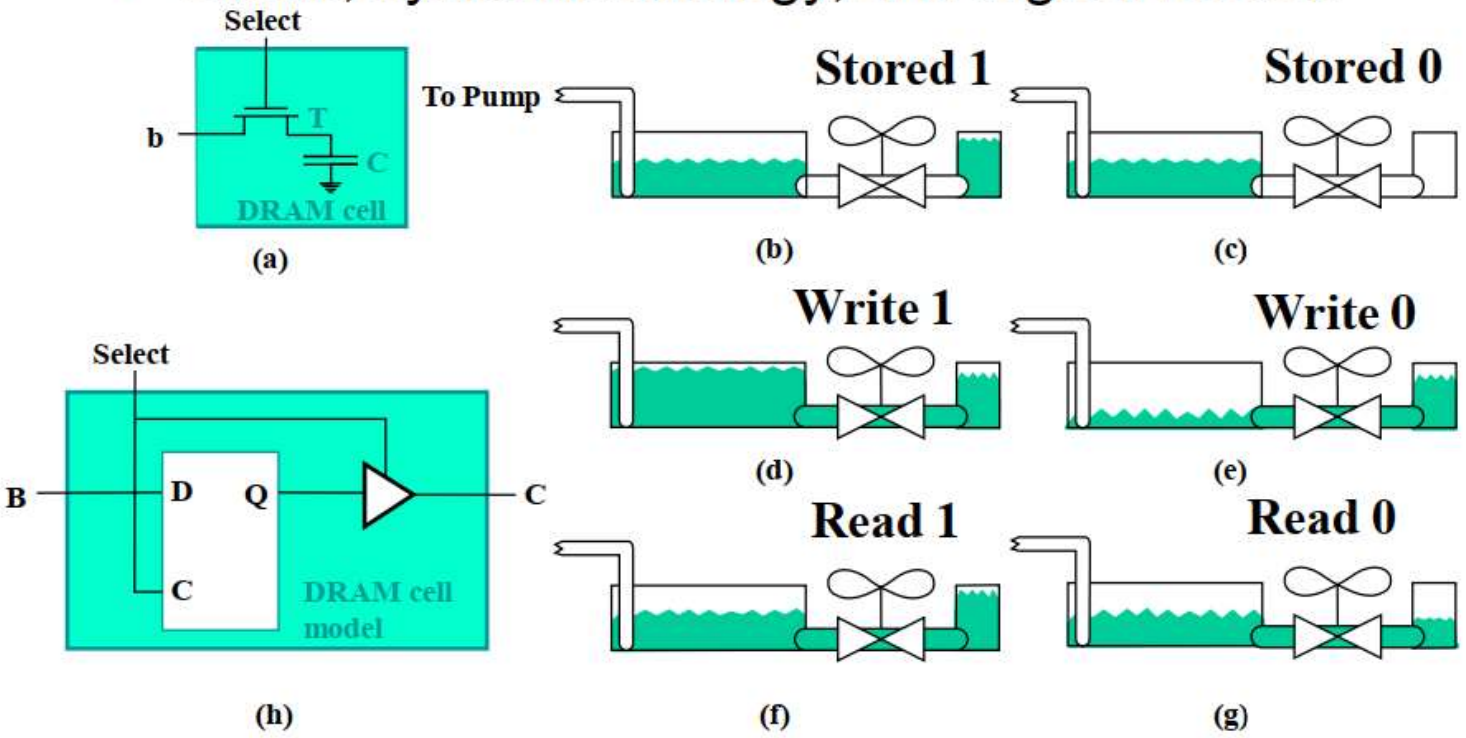


DRAM

- Basic Principle: Storage of information on capacitors.
- Charge and discharge of capacitor to change stored value
- Use of transistor as “switch” to:
  - Store charges
  - Charge or discharge

Dynamic RAM (Contd.)

- Circuit, hydraulic analogy, and logical model.



Dynamic RAM - Bit Slice

- C driven by 3-state drivers
- Sense amplifier is used to change the small voltage change on C into H or L
- In the electronics, B, C, and the sense amplifier output are connected to make destructive read into non-destructive read