Lecture two

1- Common signals for minimum and maximum modes

- $AD_0 - AD_7$ ： The address/ data bus lines are the multiplexed address data bus and contain the right most eight bit of memory address or data. The address and data bits are separated by using *ALE* signal.
- $AD_8 - AD_{15}$ ： The address/data bus lines compose the upper multiplexed address/data bus. This lines contain address bit $A_8 - A_{15}$ *and* $D_8 - D_{15}$. The address and data bits are separated by using *ALE* signal.
- A_{16}/S_3- A_{19}/S_6 The address/status bus bits are multiplexed to provide address signals A_{16} to A_{19} and also status bits $S_3$to S_6 . The address bits are separated from the status bits using the ALE signals. The status bit S_6 is always a logic 0, S_5 indicates the condition of the interrupt flag bit. The S_3 and S_4 indicate which segment register is presently being used for memory access.

1- Common signals for minimum and maximum modes for 8086

Table (1)

$S_3\ S_4$	Type of Segment Register
00	Extra segment
01	Stack segment
10	Code segment
11	Data segment

1- Common signals for minimum and maximum modes

- $\overline{BHE}/S_7$ The bus high enable (BHE) signal is used to indicate the transfer of data over the higher order ($D_8 to\ D_{15}$) data bus. It goes low for the data transfer over $D_8 to D_{15}$ and is used to derive chip select of odd address memory bank or peripherals.
- $\overline{RD}$ whenever the read signal is at logic 0 the data bus receives the data from the memory or I/O devices connected to the system.
- *READY*: This is the acknowledgement from the slow devices or memory that they have completed the data transfer operation. This signal is active high.
- *INTR*: Interrupt Request: Interrupt request is used to request a hardware interrupt of *INTR* is held high when interrupt enable flag is set, the 8086 enters an interrupt acknowledgement cycle after the current instruction has completed its execution.
- $\overline{TEST}$: This input is tested by "*WAIT*" instruction. If the *TEST* input goes low; execution will continue. Else the processor remains in an idle state.
- *NMI*- Non-maskable Interrupt: The non-maskable interrupt input is similar to *INTR* except that the *NMI* interrupt does not check for interrupt enable flag is at logic 1, i.e, *NMI* is not maskable internally by software. If *NMI* is activated, the interrupt input uses interrupt vector 2.

1- Common signals for minimum and maximum modes for 8086

- *RESET*: The reset input causes the microprocessor to reset itself. When 8086 reset, it restarts the execution from memory location *FFFF0H*. The reset signal is active high and must be active for at least four clock cycles.
- *CLK*: Clock input: The clock input signal provides the basic timing input signal for processor and bus control operation. It is asymmetric square wave with 33% duty cycle.
- VCC: Power supply for the operation of the internal circuit.
- *GND:* Ground for the internal circuit.
- $MN/\overline{MX}$: The minimum/maximum mode signal to select the mode of operation either in minimum or maximum mode configuration. Logic 1 indicates minimum mode.

2- Block Diagram of Minimum Mode Interface for 8086

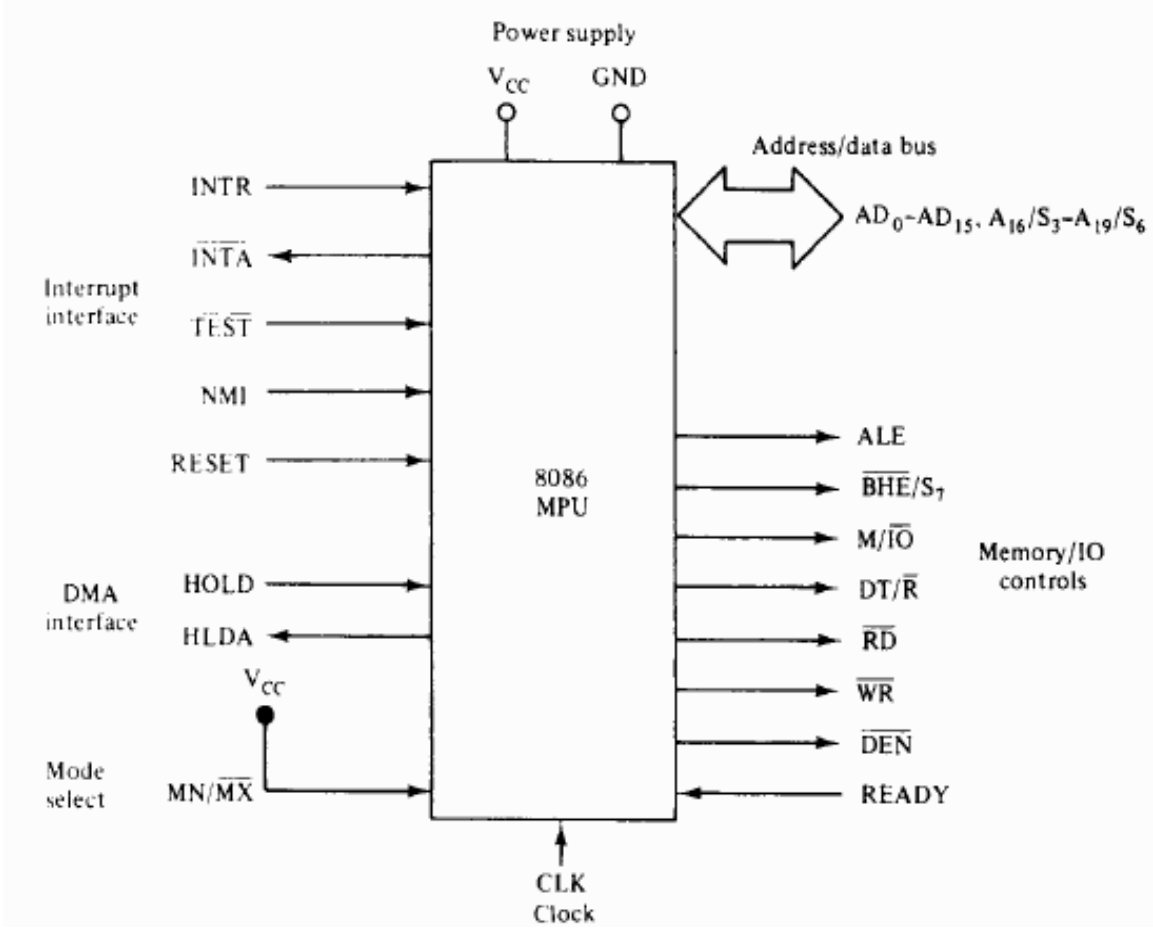


Figure (1)

2- Minimum mode signal: The following signals are for minimum mode operation of 8086.

- For minimum mode operation $MN/\overline{MX}$ connected to VCC. The description of pins in minimum mode is:-
- $\overline{INTA}$ (active low)(output). Interrupt Acknowledge. On receiving interrupt signal the processor issues an interrupt acknowledge signal.
- ALE (output). Address Latch Enable. It goes high during T1. The microprocessor sends the signal to latch the address in the latch.
- $\overline{DEN}$ (output). Data Enable. When octal bus transceiver is used, this signal acts as an output enable signal. It is active low.
- $DT/\bar{R}$ (active low)(output). Data Transmit/Receive. When octal bus transceiver is used, this signal controls the direction of data flow through the transceiver. When it is high data are sent out. When it is low data are received.

2- Minimum mode signal: The following signals are for minimum mode operation of 8086.

- $\mathrm{M}/\overline{IO}$ (active low)(output). Memory or I/O access. When it is high the CPU wants to access memory. When it is low, the CPU wants to access IO device.
- $\overline{WR}$ (active low)(output). Write When it is low the CPU performs memory or I/O write operation.
- $HLDA$ (output). Hold Acknowledge. It is used by the processor ,when it receives hold signal. When hold request is removed, HLDA goes low.
- $HOLD$ (input. Hold. When another device in the complex microcomputer system wants to use the address and the data bus, it sends a hold request through this pin.

3- Maximum mode signal: The following signals are for maximum mode operation of 8086.

- $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ Status lines: These are the status lines that reflect the type of operation being carried out by the processor. These status lines are encoded as follows:-

Table (2)

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive (In active)

3- Maximum mode signal: The following signals are for maximum mode operation of 8086.

- $\overline{LOCK}$: The lock output is used to lock peripherals off the system, i.e, the other system bus masters will be prevented from gaining the system bus.
- QS_1, QS_0- Queue status: The queue status bits shows the status of the internal instruction queue. The encoding of these signals is as follows:-
- Table (3)

QS_1	QS_0	Function
0	0	No operation, queue is idle
0	1	First byte of opcode.
1	0	Queue is empty
1	1	Subsequent byte of opcode

3- Maximum mode signal: The following signals are for maximum mode operation of 8086.

- $\overline{RQ_1}/\overline{GT_1}$ and $\overline{RQ_0}/\overline{GT_0}$ request/Grant: The request/grant pins are used by other local bus masters to force the processor to release the local bus at the end of the processors current bus cycle. These lines are bidirectional and are used to both request and grant a *DMA* operation. $\overline{RQ_0}/\overline{GT_0}$ is having higher priority than $\overline{RQ_1}/\overline{GT_1}$.

3-Block diagram of maximum mode signals

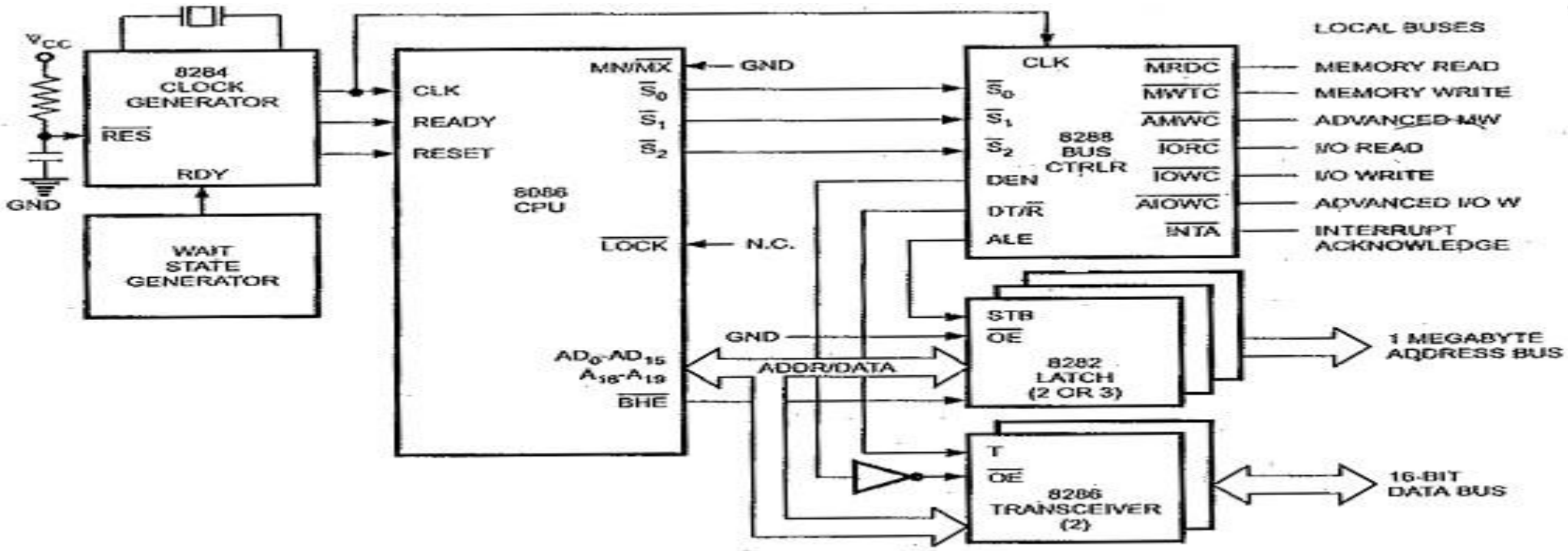
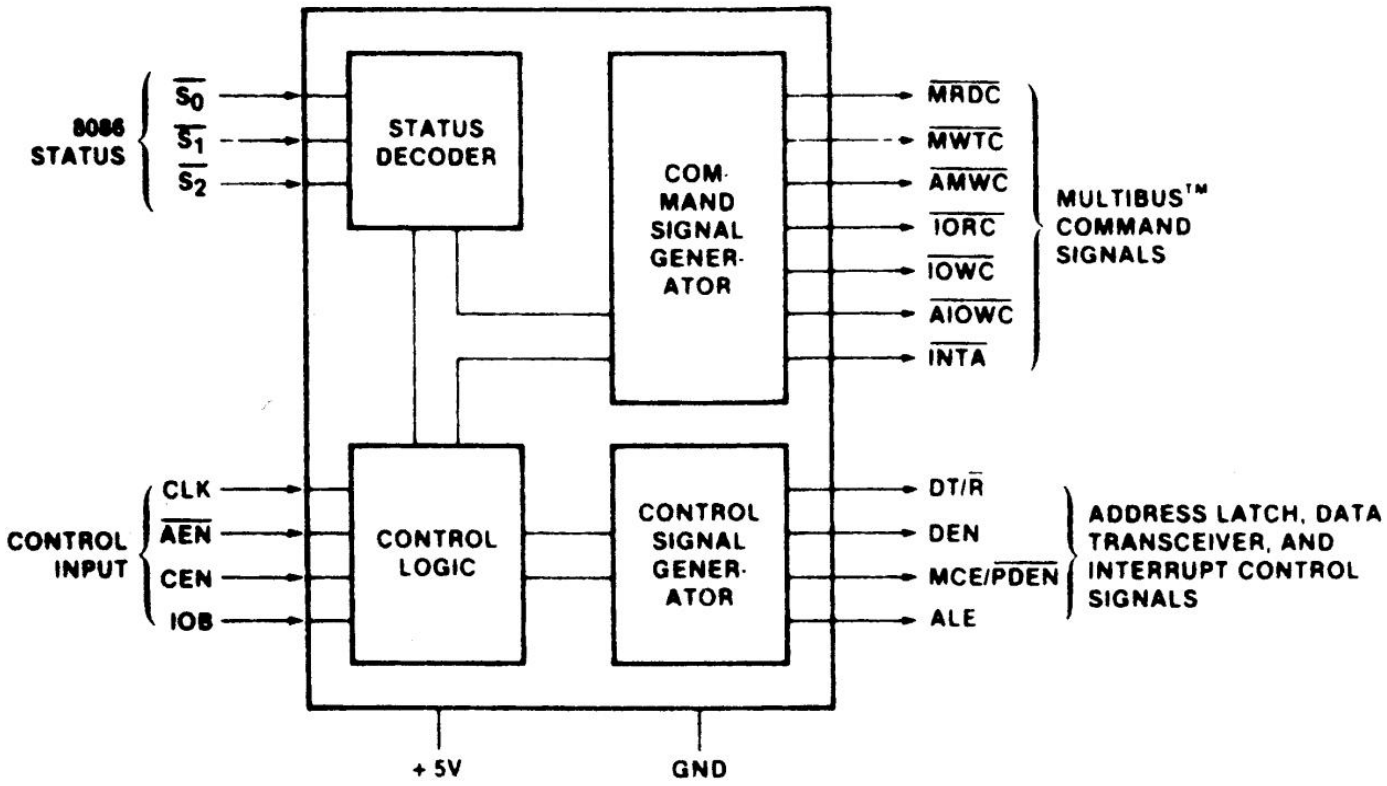


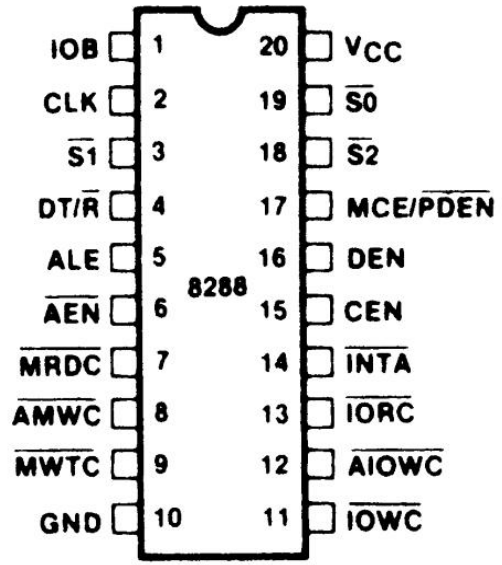
Fig. 10.8 Typical maximum mode configuration

Figure (2) Block diagram of maximum mode signals

3-Maximum mode signals



(a)



(b)

Figure (3) 8288 bus controller

3-Maximum mode signals

8288 Bus Controller *Pin Functions*

$\boldsymbol{ALE}$

•The **address latch enable** output is used to demultiplex the address/data bus.

$\overline{DEN}$

•The **data bus enable** pin controls the bidirectional data bus buffers in the system.

$DT/\bar{R}$

•**Data transmit/receive** signal output to control direction of the bidirectional data bus buffers.

Maximum mode signals

$\overline{AEN}$

•The **address enable** input causes the 8288 to enable the memory control signals.

CEN

•The **control enable** input enables the command output pins on the 8288.

IOB

•The **I/O bus mode** input selects either I/O bus mode or system bus mode operation.

$\overline{AIOWC}$

•**Advanced I/O write** is a command output to an advanced I/O write control signal.

$\overline{IORC}$

•The **I/O read command** output provides I/O with its read control signal.

Maximum mode signals

$\overline{IOWC}$

•The **I/O write command** output provides I/O with its main write signal.

$\overline{AMWT}$

•**Advanced memory write** control pin provides memory with an early/advanced write signal.

$\overline{MWTC}$

•The **memory write** control pin provides memory with its normal write control signal.

$\overline{MRDC}$

•The **memory read** control pin provides memory with a read control signal .

$\overline{INTA}$

•The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

4- 8086 Minimum mode system operation

- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system. The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.
- Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.
- The general system organization is shown in below figure.
- The latches are generally buffered output D-type flip-flops, like, 74LS373 or 8282.

4- 8086 Minimum mode system operation with timing diagrams:

- They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.
- Since it has 20 address lines and 16 data lines, the 8086 CPU requires three octal address latches and two octal data buffers for the complete address and data separation.
- Transreceivers are the bidirectional buffers and sometimes they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signal.
- They are controlled by two signals, namely, $\overline{DEN}$ and $\mathrm{DT}/\overline{R}$. The $\overline{DEN}$ signal indicates that the valid data is available on the data bus, while $\mathrm{DT}/\overline{R}$ indicates the direction of data, i.e. from or to the processor.
- The system contains memory for the monitor and users program storage. Usually, EPROMS are used for monitor storage, while RAMs for users program storage.
- A system may contain I/O devices for communication with the processor as well as some special purpose I/O devices.

4- 8086 Minimum mode system operation

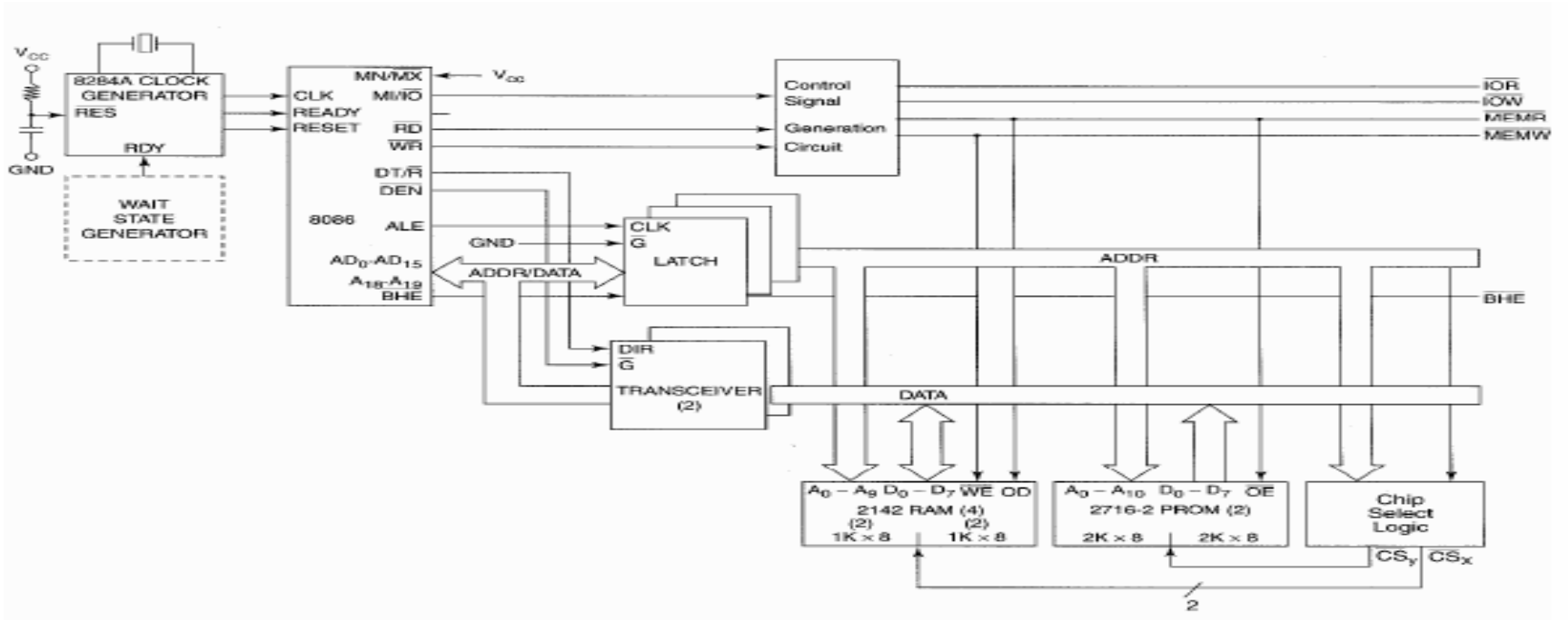


Figure (4) Block diagram of minimum mode system

5- Clock Generator

- The clock generator generates the clock from the crystal oscillator and then shapes it and divides to make it more precise so that it can be used as an accurate timing reference for the system.
- The clock generator also synchronizes some external signals with the system clock.
- The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.
- The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.

5- Clock Generator

SYSTEM CLOCK

To synchronize the internal and external operations of the microprocessor a *clock* (CLK) input signal is used. The CLK can be generated by the 8284 clock generator IC.

The 8086 is manufactured in three speeds: 5 MHz, 8 MHz and 10 MHz.

For 8086, we connect either a 15, 24 or 30-MHz crystal between inputs X1 and X2 of the clock chip (see Fig. (4)).

The *fundamental crystal frequency* is divided by 3 within the 8284 to give either a 5, 8 or 10 MHz clock signal, which is directly connected to the CLK input of the 8086.

5- Clock Generator

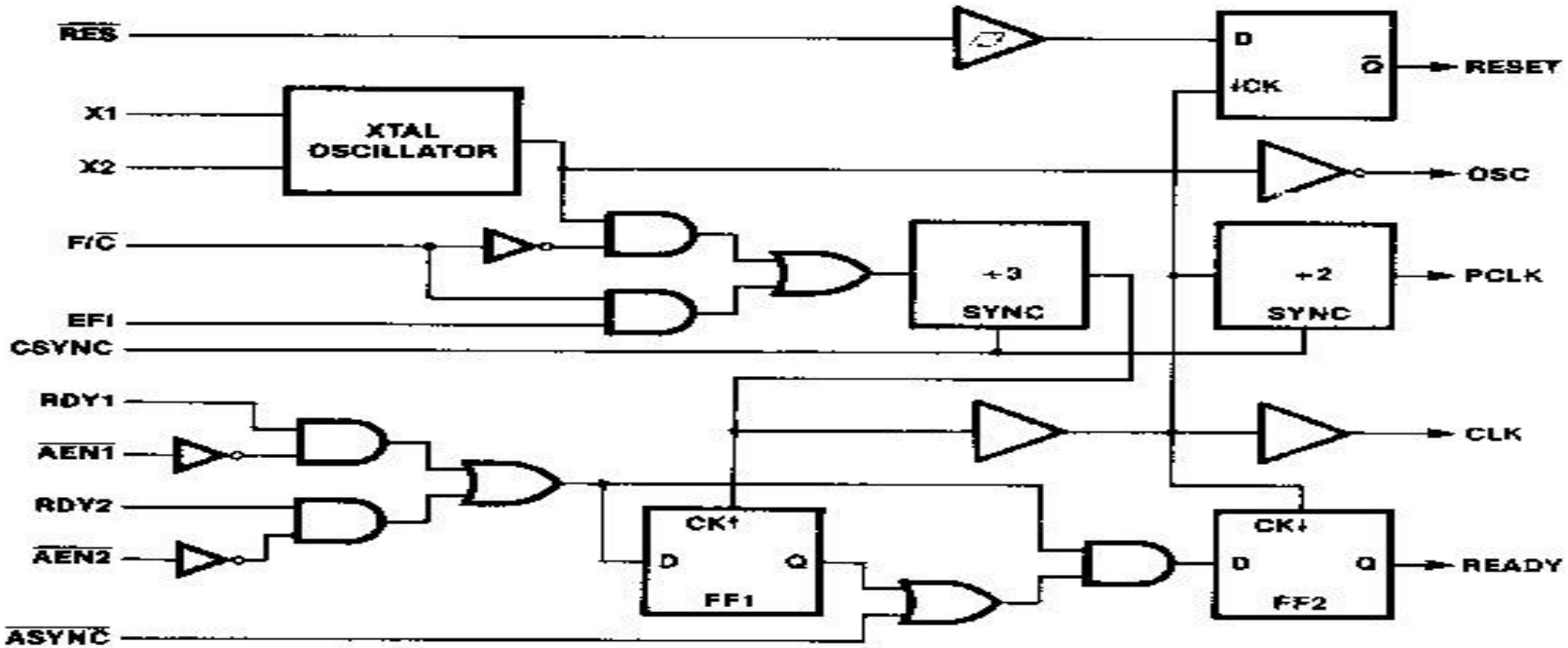


Figure (4) Internal structure of clock generator

5- Clock Generator

- The clock generator (8284A) and the 8086 and 8088 microprocessors illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.

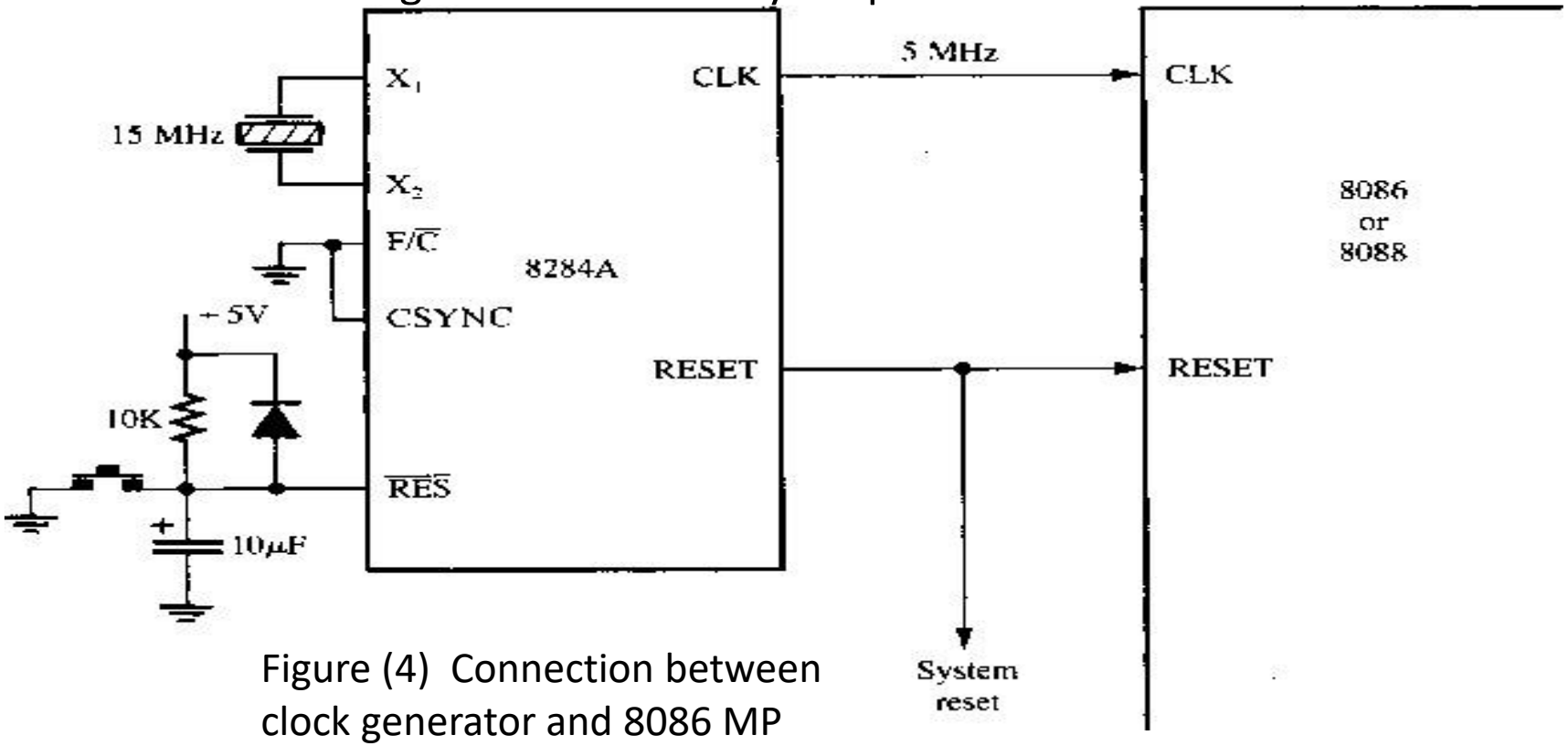


Figure (4) Connection between clock generator and 8086 MP

5- Clock generator

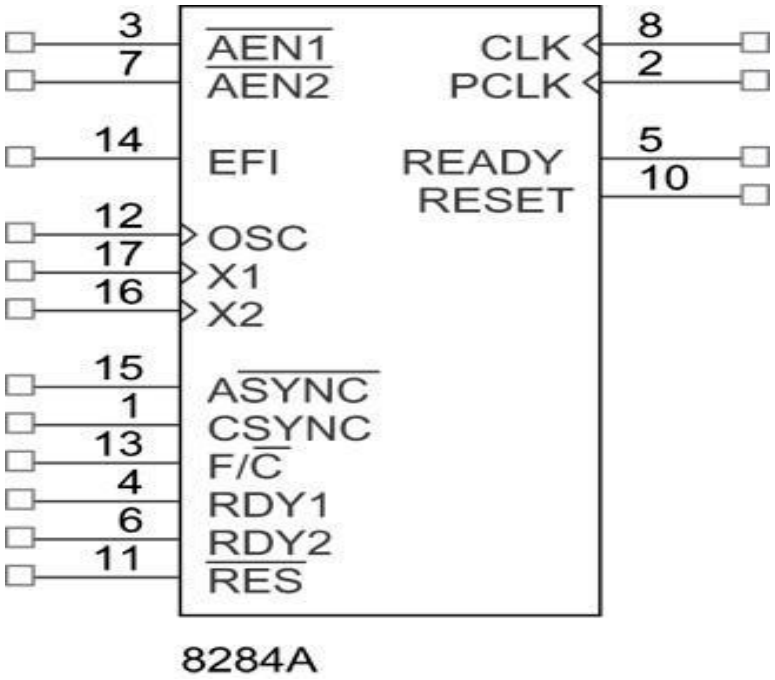


Figure (5) pin-out of the 8284A clock generator

6- Minimum mode 8086 memory Interface

- Figure (6) shows the block diagram of minimum mode memory interface.

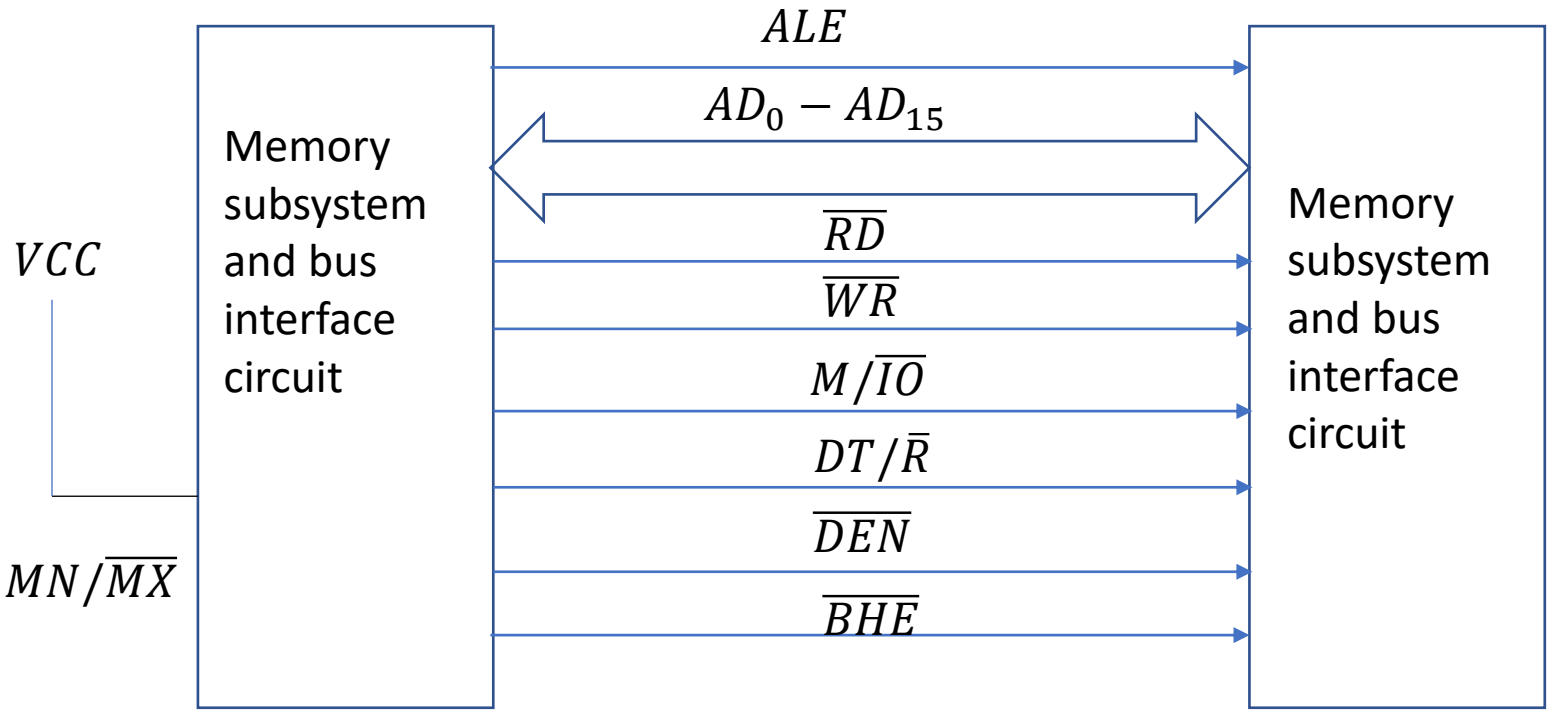


Figure (6) block diagram for minimum mode 8086 memory interface

6- Minimum mode 8086 memory Interface

- The control signals provided to support the interface to memory subsystems are ALE , $\overline{RD}$, $\overline{WR}$, $\mathrm{M}/\overline{IO}$, $\overline{DEN}$,$\overline{BHE}$, $\mathrm{DT}/\overline{R}$.
- When ALE (address latch enable) is logic one, it signals that the valid address is on the bus. This address can be latched in external circuitry on the 1-to-0 edge of the pulse at ALE.
- $\mathrm{M}/\overline{IO}$ AND $\mathrm{DT}/\overline{R}$ tells external circuits whether memory or I/O is taking place over the bus and whether 8086 transmit or receive data over the bus.
- $\overline{BHE}$ (bank high enable) is used as memory enable signal for the most significant byte, half of the data bus, $D_8\ to\ D_{15}$.
- The signals $\overline{RD}$ $(read)$, $\overline{WR}$(write) identify that read or write bus cycle in the progress.
- $\overline{DEN}$ (data enable). It is enabled external device to supply data to microprocessor.

7- Maximum mode 8086 memory interface

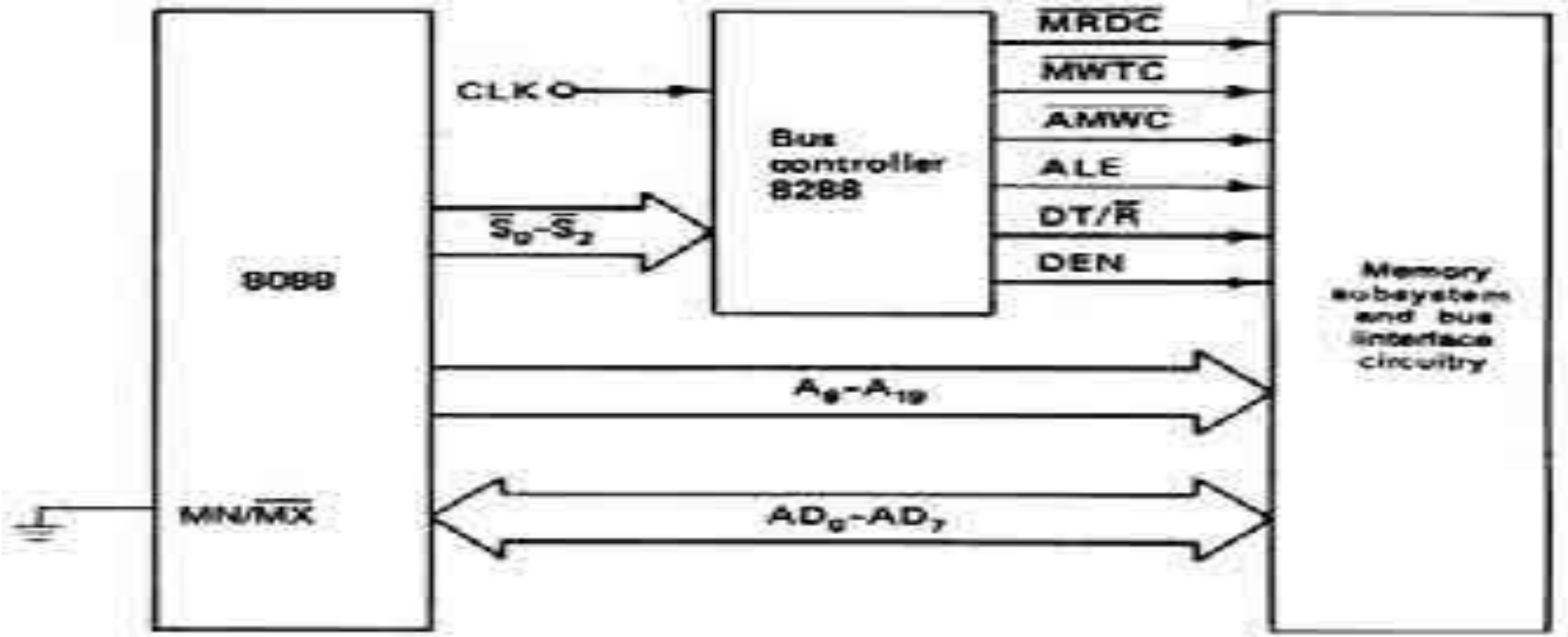


Figure (7) block diagram for maximum mode 8086 memory interface

7- Maximum mode 8086 memory interface

Figure (7) show block diagram of maximum mode memory interface.

- In maximum mode the 8086 not directly provides all control signal to support the memory interface.
- Instead, an external Bus Controller (8288) provides memory commands and control signals as shown in table (2) .

8- A fully buffered 8088 microprocessor

- Figure (8) depicts a fully buffered 8088 microprocessor.
- –a fully buffered 8088 system requires two 74LS244s, one 74LS245, and two 74LS373s
- Direction of the 74LS245 is controlled by the $DT/\bar{R}$ signal.
- –enabled and disabled by the $\overline{DEN}$ signal

8- A fully buffered 8088 microprocessor

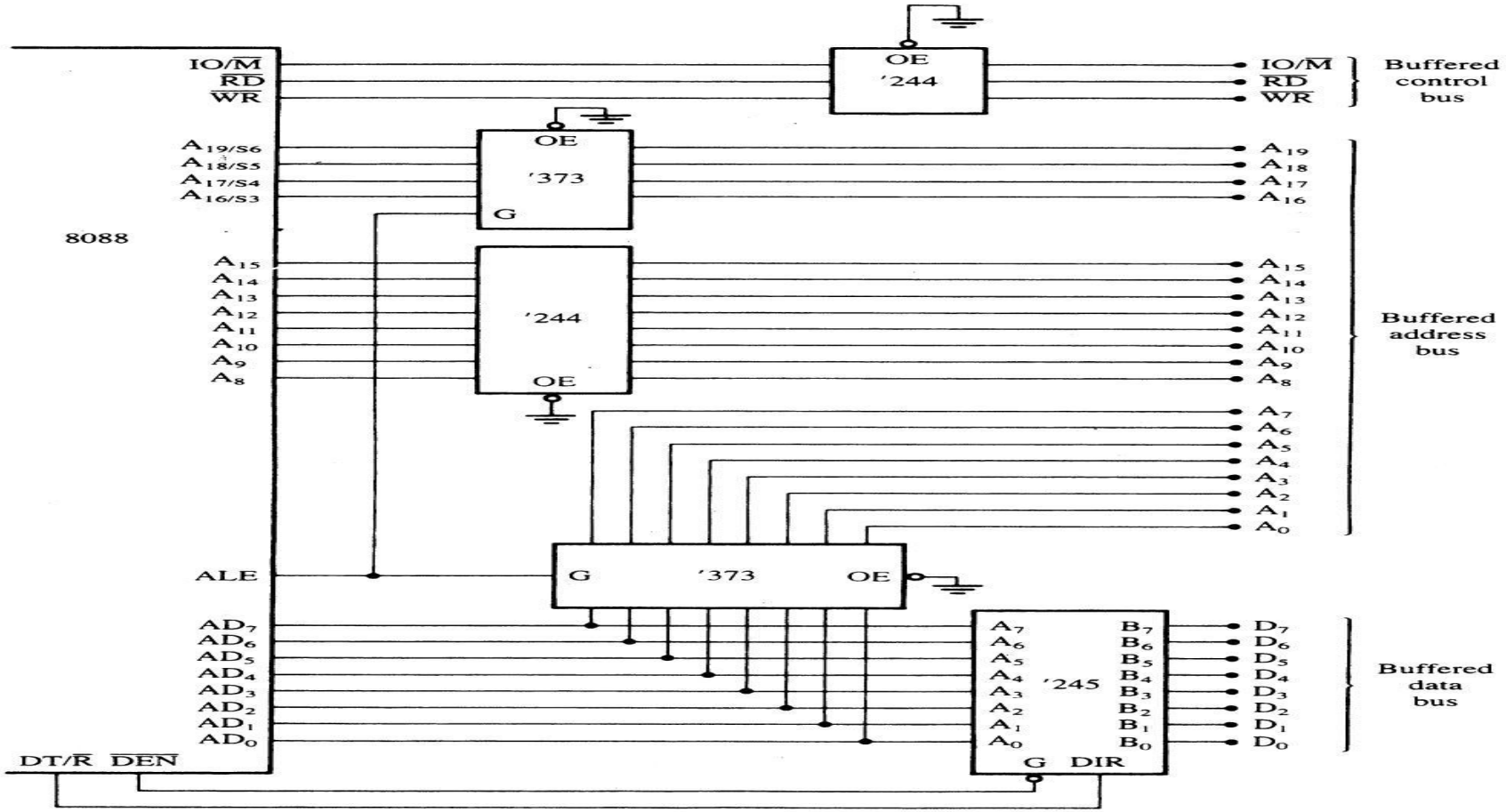


Figure (8) fully buffered 8088 microprocessor

9- A fully buffered 8086 microprocessor

- Figure (9) illustrates a fully buffered 8086.
  –a fully buffered 8086 system requires one 74LS244, two 74LS245s, and three 74LS373s

•8086 requires one more buffers than 8088 because of the extra eight data bus connections, D15–D8.

•It also has a $\overline{BHE}$ signal that is buffered for memory-bank selection.

9-A fully buffered 8086 microprocessor.

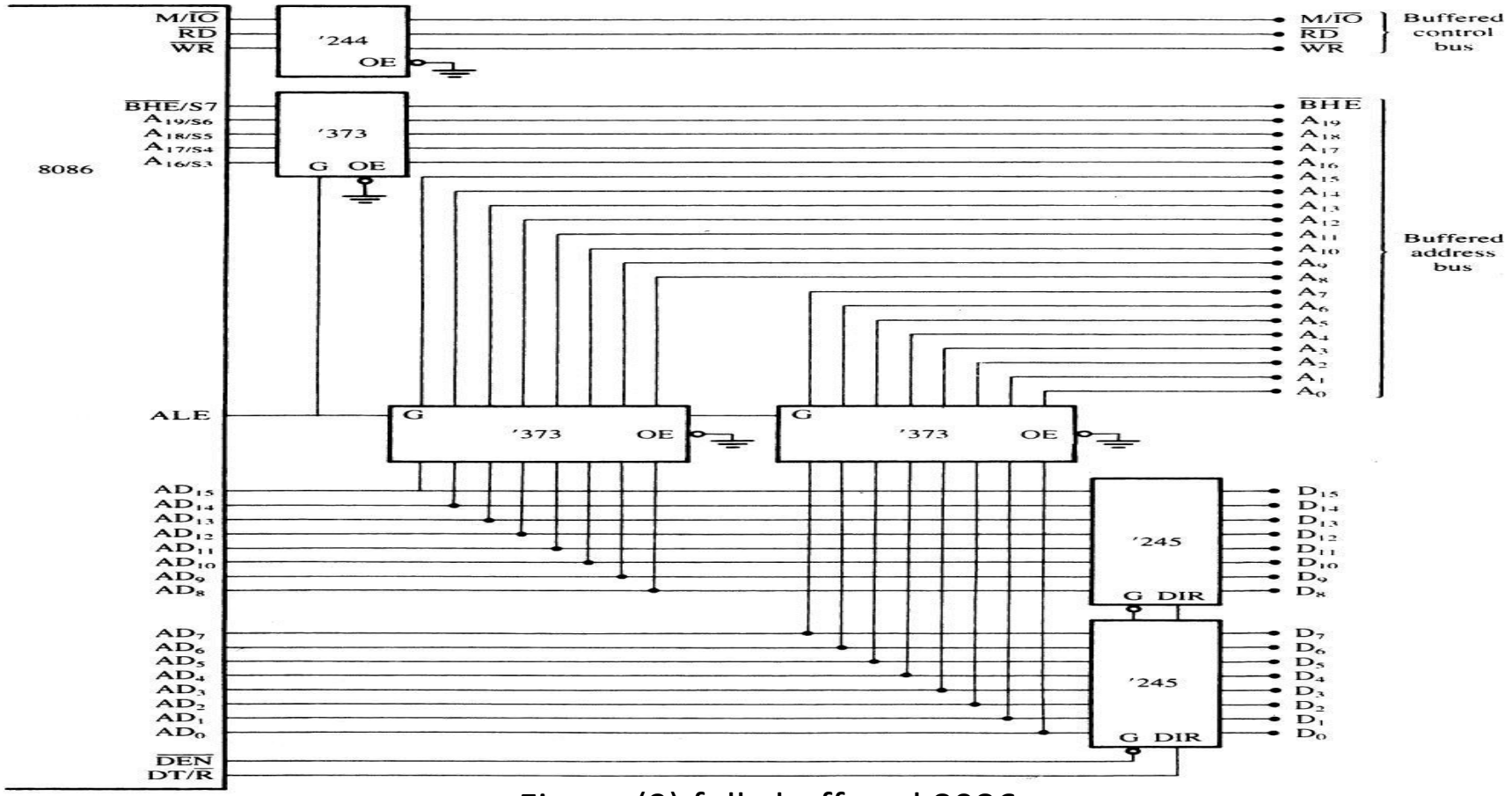


Figure (9) fully buffered 8086 microprocessor

10- Comparison between minimum and maximum modes

- Minimum mode is obtained by connecting the mode selection $MN/\overline{MX}$ pin to +5.0 V,
  –maximum mode selected by grounding the pin
- The mode of operation provided by minimum mode is similar to that of the 8085A
  –the most recent Intel 8-bit microprocessor
- Maximum mode is designed to be used whenever a coprocessor exists in a system.
  –maximum mode was dropped with 80286

10- Comparison between minimum and maximum modes

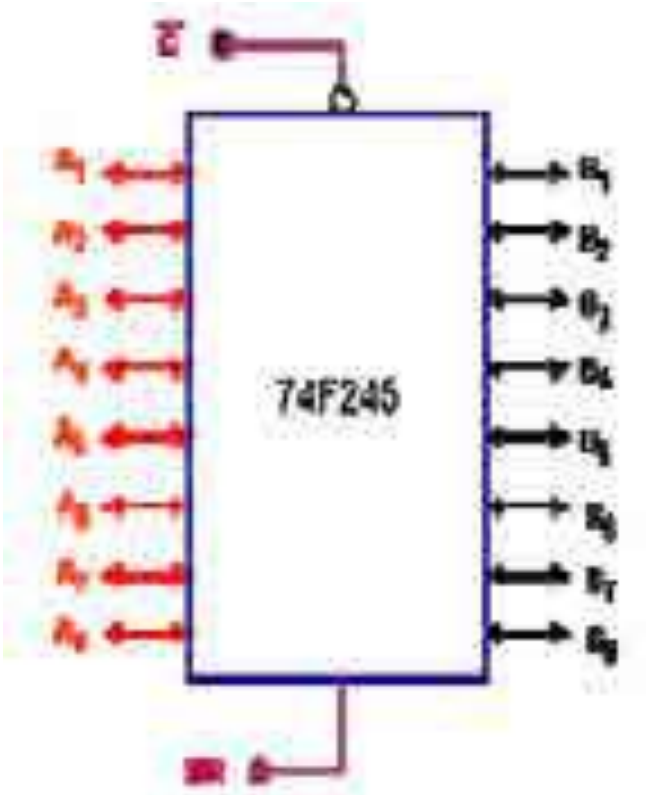
- Least expensive way to operate 8086/8088.

  –because all control signals for the memory & I/O are generated by the microprocessor

•Control signals are identical to Intel 8085A.

•The minimum mode allows 8085A 8-bit peripherals to be used with the 8086/8088 without any special considerations.

The block and circuit diagram of the 8-bit Data bus transceiver buffer IC.



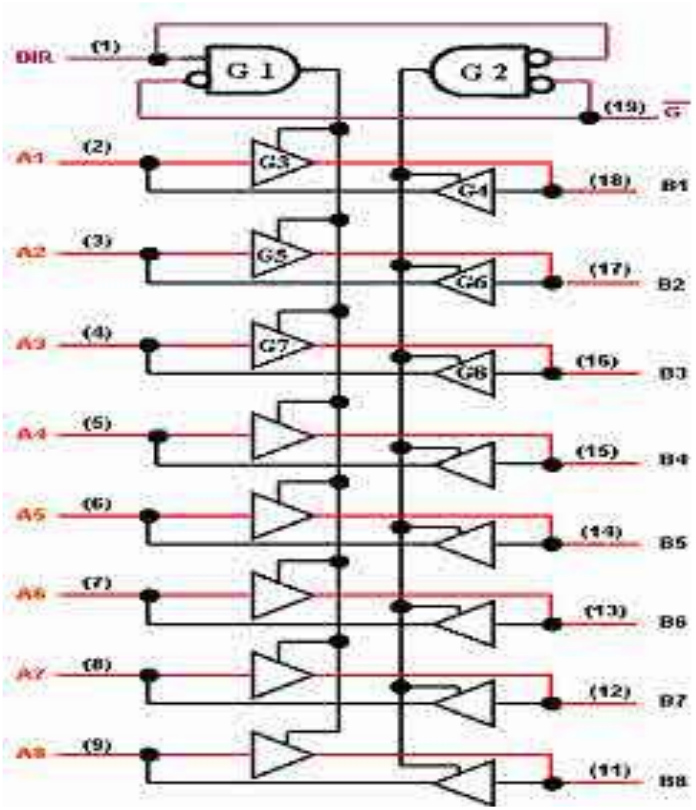


Figure (10) 74LS245

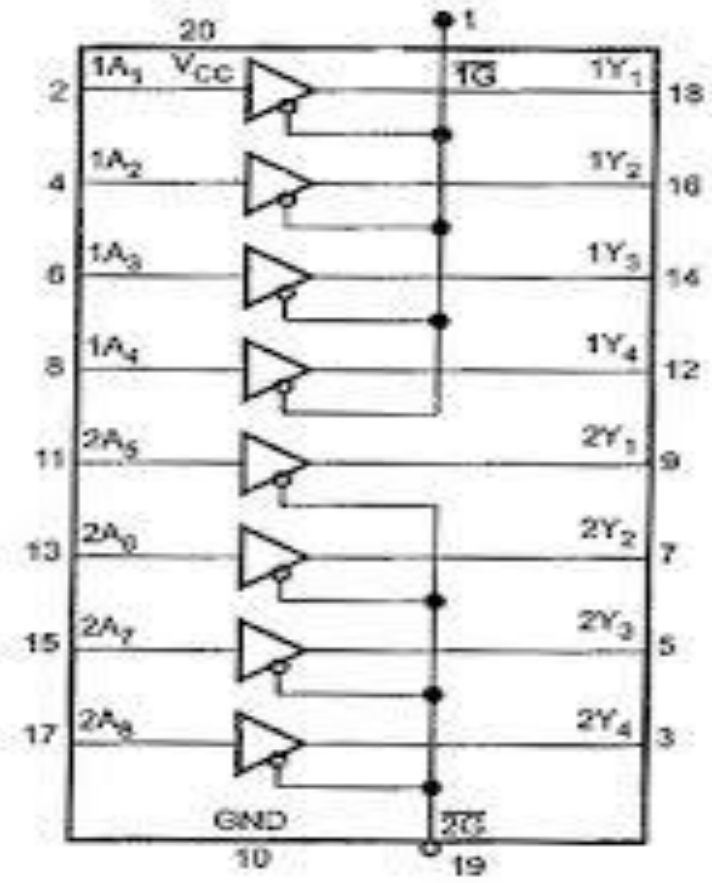


Fig. 4.10 Logic diagram of the 74LS244

74LS244、74F244、74ALS244、74HCT244、74S244、74HC244、74C244 八缓冲器/线驱动器/线接收器（三态）

当$\overline{1G}$、$\overline{2G}$是H时，Y为高阻抗；当$\overline{1G}$、$\overline{2G}$是L时，Y=A。

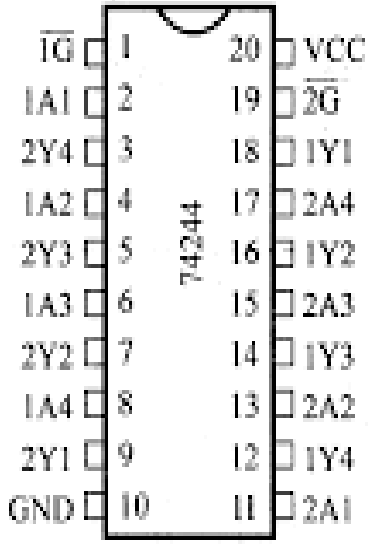


Figure (11) 74LS244

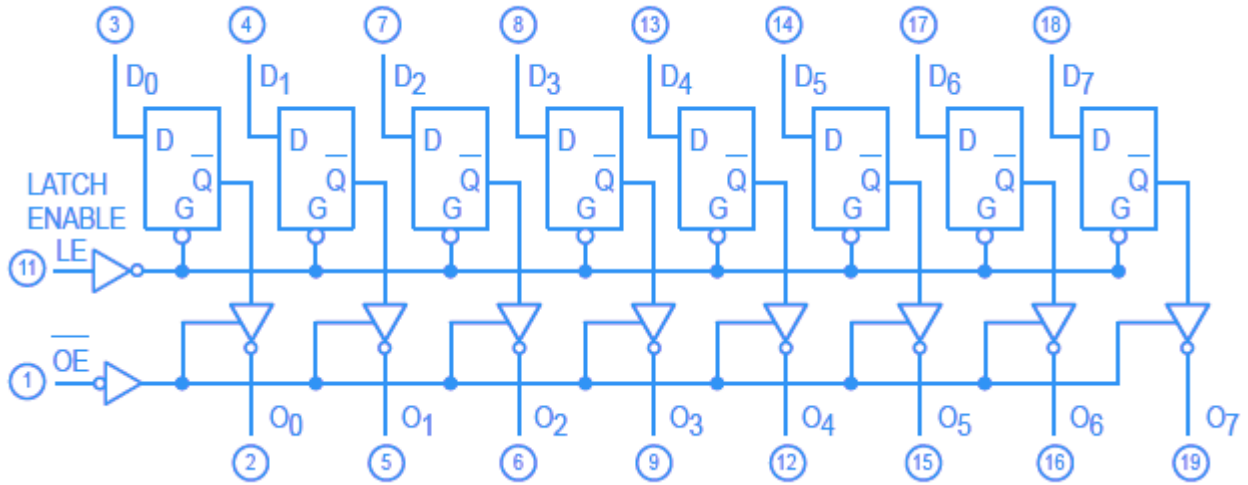


Figure (12) 74LS373