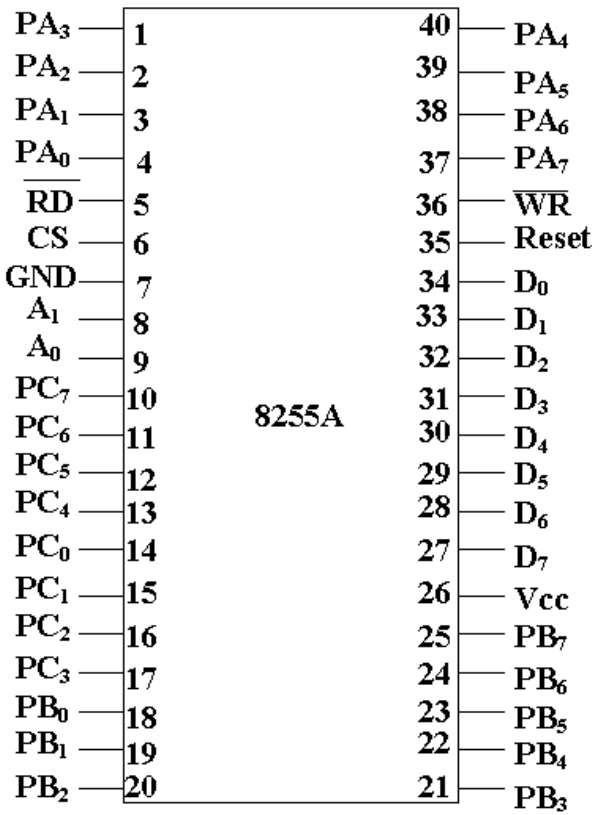
PPI




8255A Pin Configuration

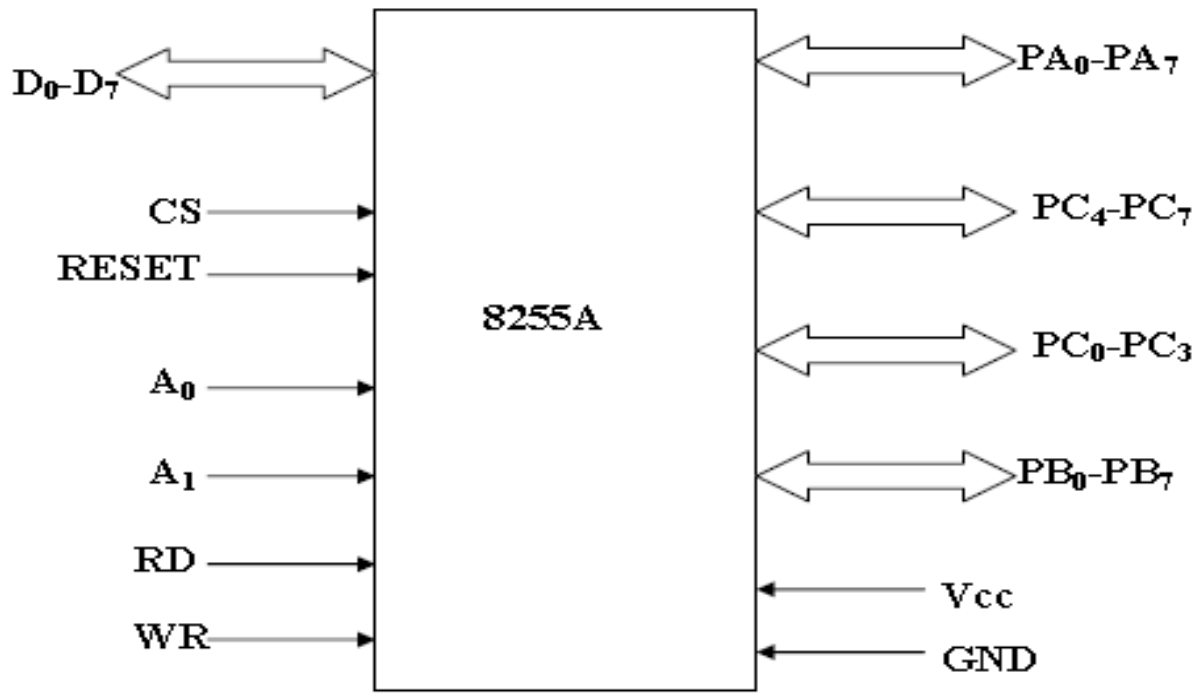


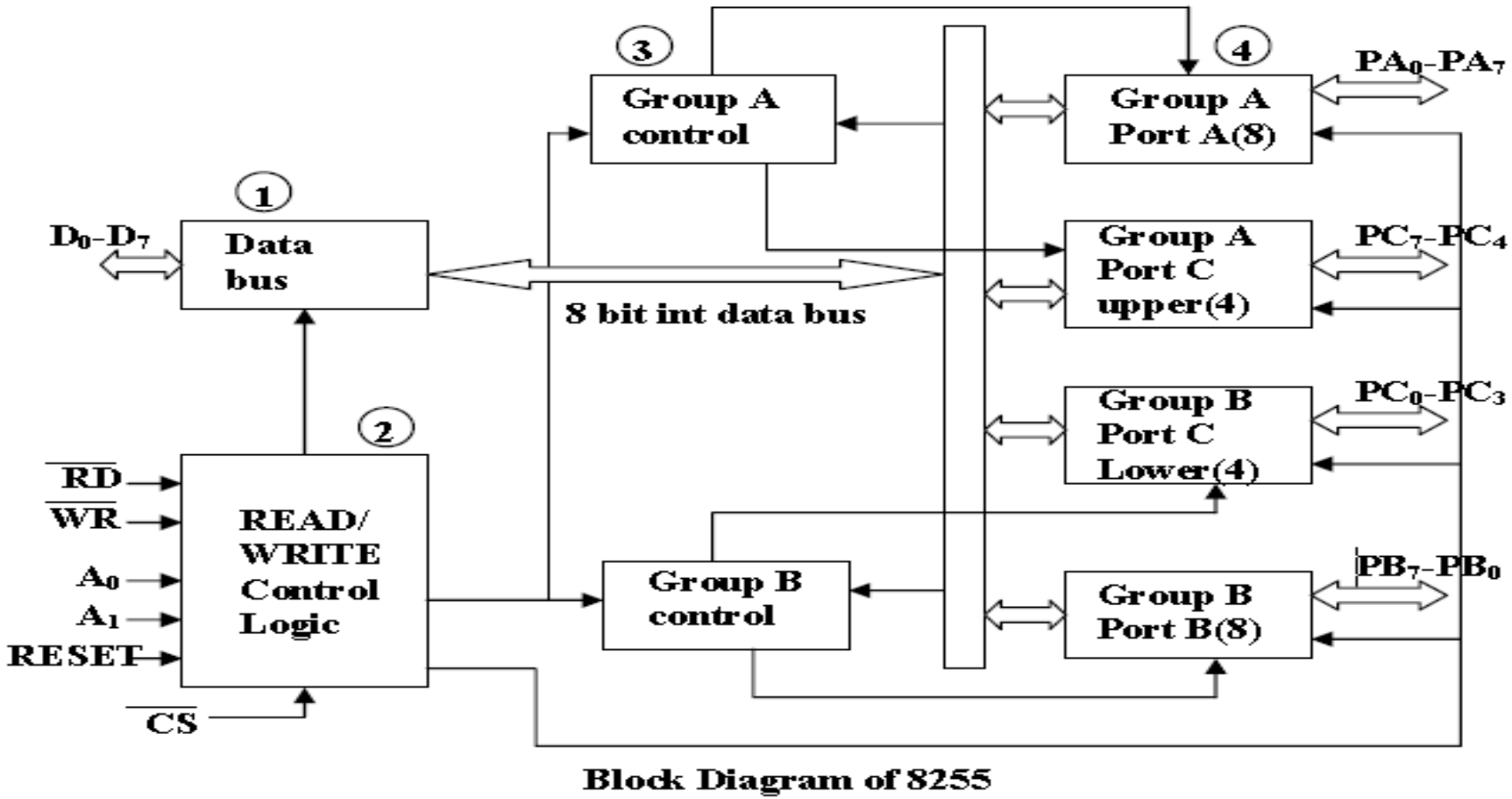

Figure (1)

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Input (Read) cycle |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Port A to Data bus |
| 0 | 1 | 0 | 0 | 1 | Port B to Data bus |
| 0 | 1 | 0 | 1 | 0 | Port C to Data bus |
| 0 | 1 | 0 | 1 | 1 | CWR to Data bus |

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $A_1$ | $A_0$ | Output (Write) cycle |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | Data bus to Port A |
| 1 | 0 | 0 | 0 | 1 | Data bus to Port B |
| 1 | 0 | 0 | 1 | 0 | Data bus to Port C |
| 1 | 0 | 0 | 1 | 1 | Data bus to CWR |

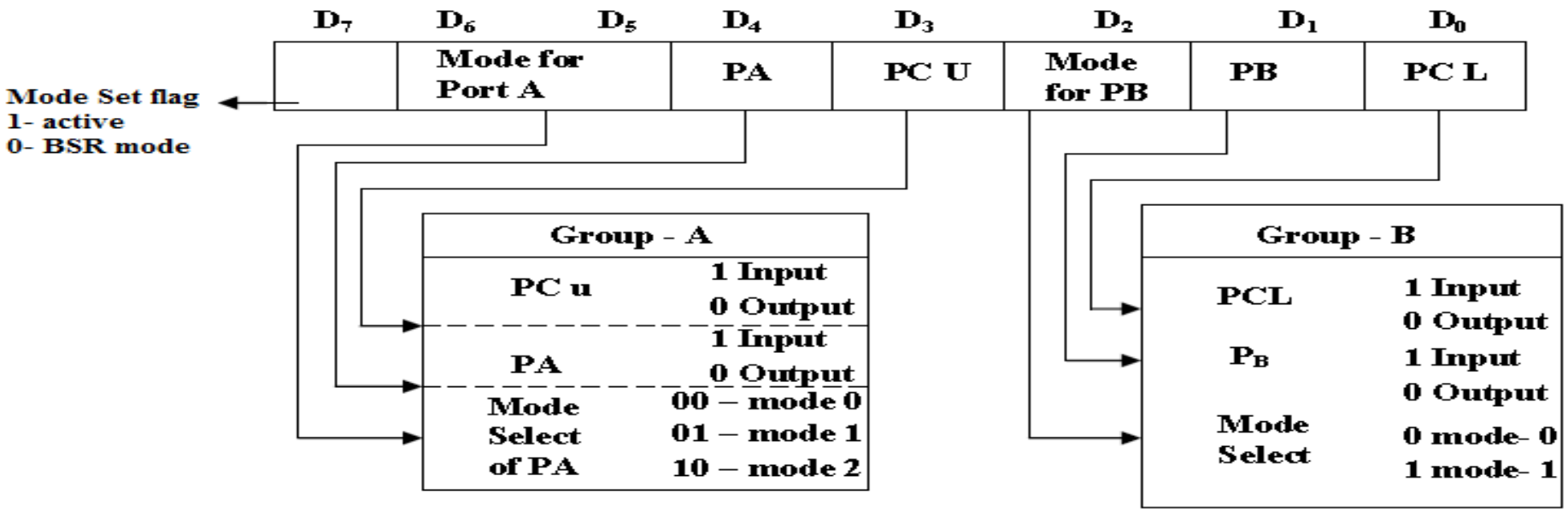
**Block Diagram of 8255 (Architecture):**

1. Data bus buffer.
2. Read Write control logic.
3. Group A and Group B controls.
4. Port A, B and C .



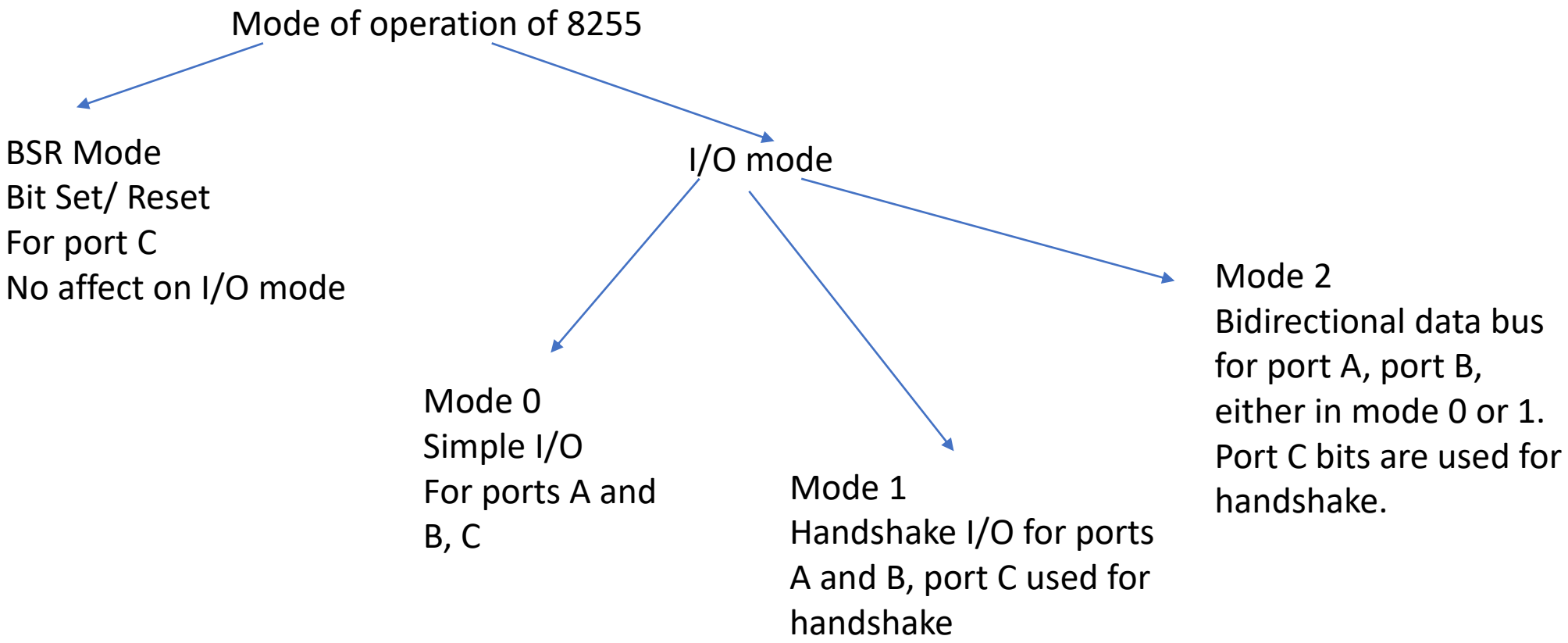

Block Diagram of 8255

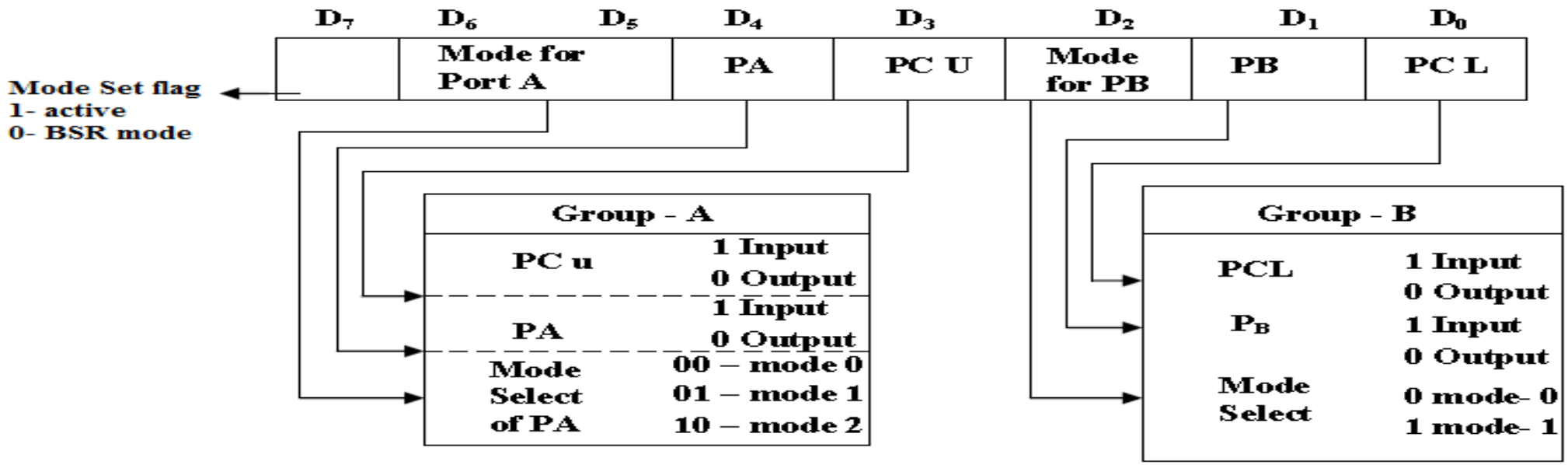
Figure (2)




Control Word Format of 8255

Figure (3)


Mode of operation of 8255
BSR Mode
Bit Set/ Reset
For port C
No affect on I/O mode
I/O mode
Mode 0
Simple I/O
For ports A and
B, C
Mode 1
Handshake I/O for ports
A and B, port C used for
handshake
Mode 2
Bidirectional data bus
for port A, port B,
either in mode 0 or 1.
Port C bits are used for
handshake.

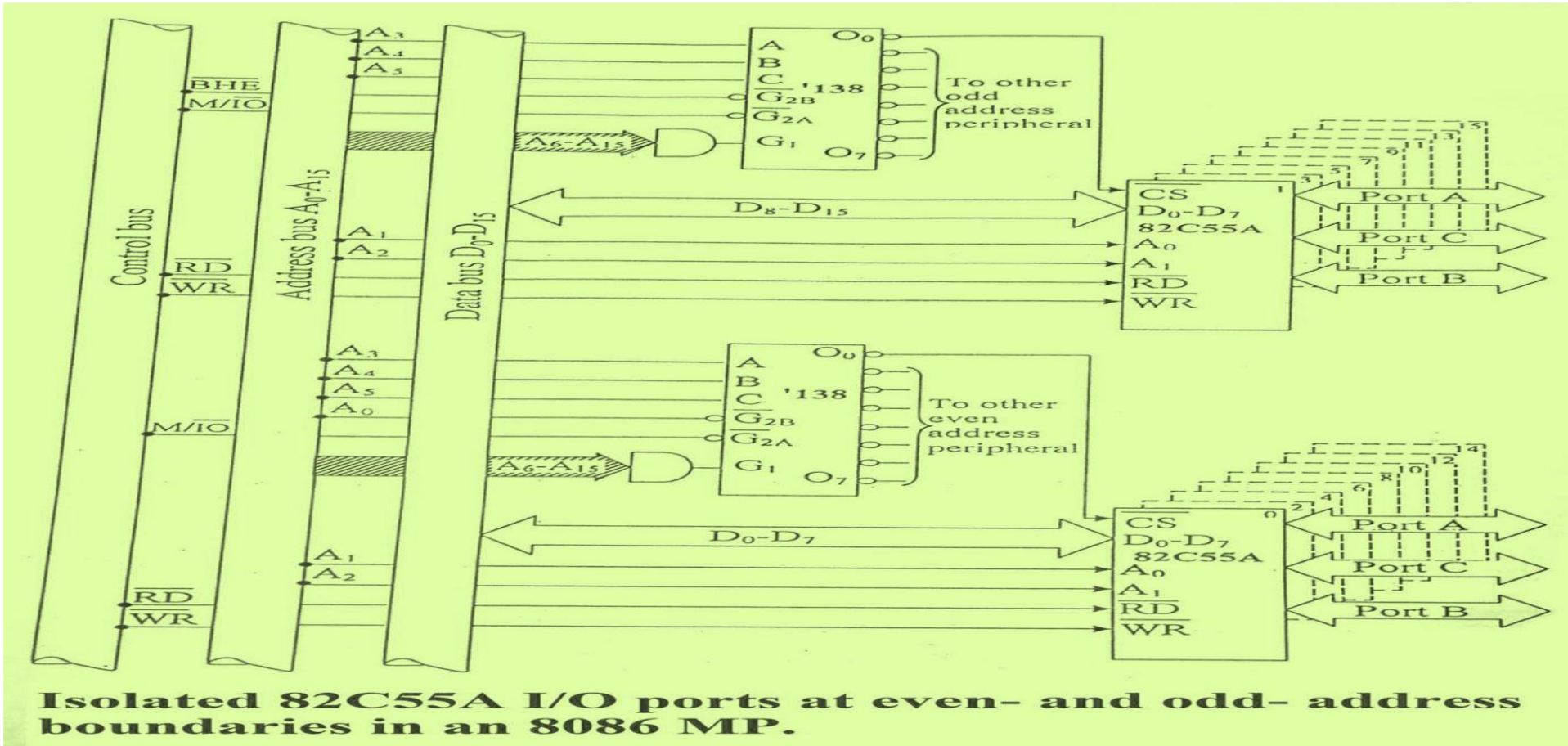



**Control Word Format of 8255**

Example1: what is the mode and I/O configuration for ports A,B and C of an 82C55A after its control register is loaded with 82 H.

1000 0010

D0 PCL =0 Output
D1 PB= 1 Input
D2 Mode for PB mode 0
D3 PCU =0 Output
D4  PA =0 output
D5D6 =00 PA mode 00
D7=1 I/O




**Isolated 82C55A I/O ports at even- and odd- address boundaries in an 8086 MP.**

Figure (4)