# Interrupts

# Interrupts in 8086 microprocessor

- An interrupt is the method of processing the microprocessor by peripheral device.
- An interrupt is used to cause a temporary halt in the execution of program.
- Microprocessor responds to the interrupt with an interrupt service routine, which is short program or subroutine that instructs the microprocessor on how to handle the interrupt

- Whenever an interrupt occurs the processor completes the execution of the current instruction and starts the execution of an Interrupt Service Routine (ISR) or Interrupt Handler. ISR is a program that tells the processor what to do when the interrupt occurs. After the execution of ISR, control returns back to the main routine where it was interrupted.

Processor can be interrupted by following ways:

- By an external signal generated by a peripheral.
- By an internal signal generated by a special instruction in the program
- By an internal signal generated due to an exceptional condition which occurs while executing an instruction.

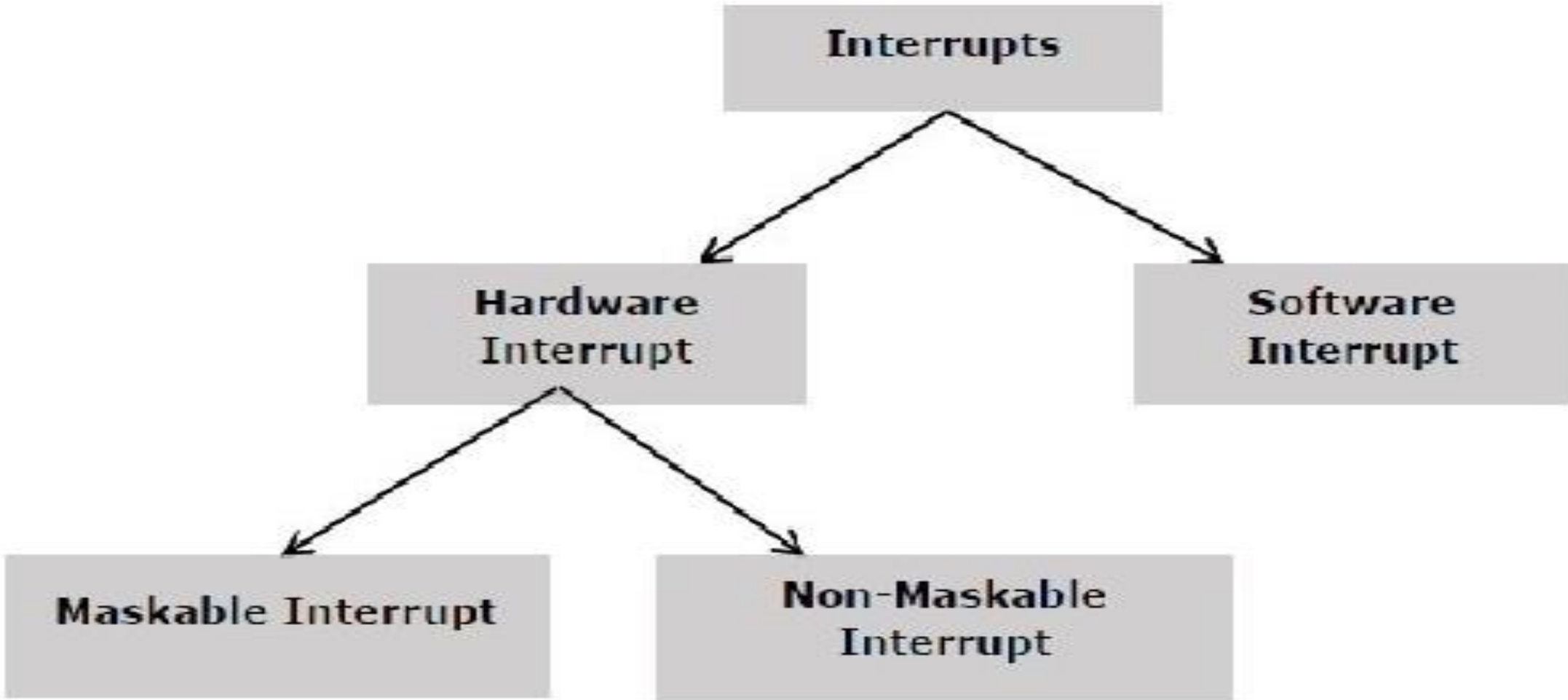
- There are two basic type of interrupt, maskable and non-maskable,
- **nonmaskable**

  nonmaskable interrupt requires an immediate response by microprocessor, it usually used for serious circumstances like power failure.

- **A maskable**

  maskable interrupt is an interrupt that the microprocessor can ignore depending upon some predetermined upon some predetermined condition defined by status register.

# Types of Interrupts in 8086



# Hardware Interrupts (External Interrupts)

The Intel microprocessors support hardware interrupts through:

- Two pins that allow interrupt requests, INTR and NMI
- One pin that acknowledges, INTA, the interrupt requested on INTR. INTR and NMI
- INTR is a maskable hardware interrupt. The interrupt can be enabled/disabled using STI/CLI instructions or using more complicated method of updating the FLAGS register with the help of the POPF instruction.

NMI is a non-maskable interrupt. Interrupt is processed in the same way as the INTR interrupt. Interrupt type of the NMI is 2, i.e. the address of the NMI processing routine is stored in location 0008h. This interrupt has higher priority than the maskable interrupt.

– Ex: NMI, INTR.

# NON-MASKABLE INTERRUPT (NMI)

- The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine.

- The NMI is edge triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

# MASKABLE INTERRUPT

- The hardward vectored interrupts are classified into maskable and non-maskable interrupts.
- Masking-preventing the interrupt from disturbing the main program.
- When an interrupt is masked the processor will not accept the interrupt signal.

| Maskable | Non-maskable |
| --- | --- |
| When a maskable interrupt occurs it can be handled after the execution of the current instruction | When nonmaskable interrupts occurs, the current instruction and status is stored in stack for the cpu to handled the interrupt. |
| Used for lower priority tasks | Used for higher priority tasks |
| It is used to interface peripherals | It is used for emergency purposes like power failure |
| It can be masked off or made pending<br><br>Response time is high | It cannot be masked off or made pending<br><br>Response time is low |

## Dedicated interrupts of 8086:

The following are the various types of interrupts:

- **Type 0** interrupts: This interrupt is also known as the divide by zero interrupt. For cases where the quotient becomes particularly large to be placed / adjusted an error might occur.
- **Type 1** interrupts: This is also known as the single step interrupt. This type of interrupt is primarily used for debugging purposes in assembly language.
- **Type 2** interrupts: also known as the non-maskable NMI interrupts. These type of interrupts are used for emergency scenarios such as power failure.

- **Type 3** interrupts: These type of interrupts are also known as breakpoint interrupts. When this interrupt occurs a program would execute up to its break point.

-**Type 4** interrupts: Also known as overflow interrupts is generally existent after an arithmetic operation was performed

- Procedures are groups of instructions that perform one task and are used from any point in a program. The CALL instruction links to a procedure and the RET instruction returns from a procedure. In assembly language, the PROC directive defines the name and type of procedure. The ENDP directive declares the end of the procedure.
- The CALL instruction is a combination of a PUSH and a JMP instruction. When CALL executes, it pushes the return address on the stack and then jumps to the procedure. A near CALL places the contents of IP on the stack, and a far CALL places both IP and CS on the stack.
- Interrupts are either software instructions similar to CALL or hardware signals used to call procedures. This process interrupts the current program and calls a procedure. After the procedure, a special IRET instruction returns control to the interrupted software.

- The interrupt enable flag (I) controls the INTR pin connection on the microprocessor. If the STI instruction executes, it sets I to enable the INTR pin. If the CLI instruction executes, it clears I to disable the INTR pin.