Computer Interface

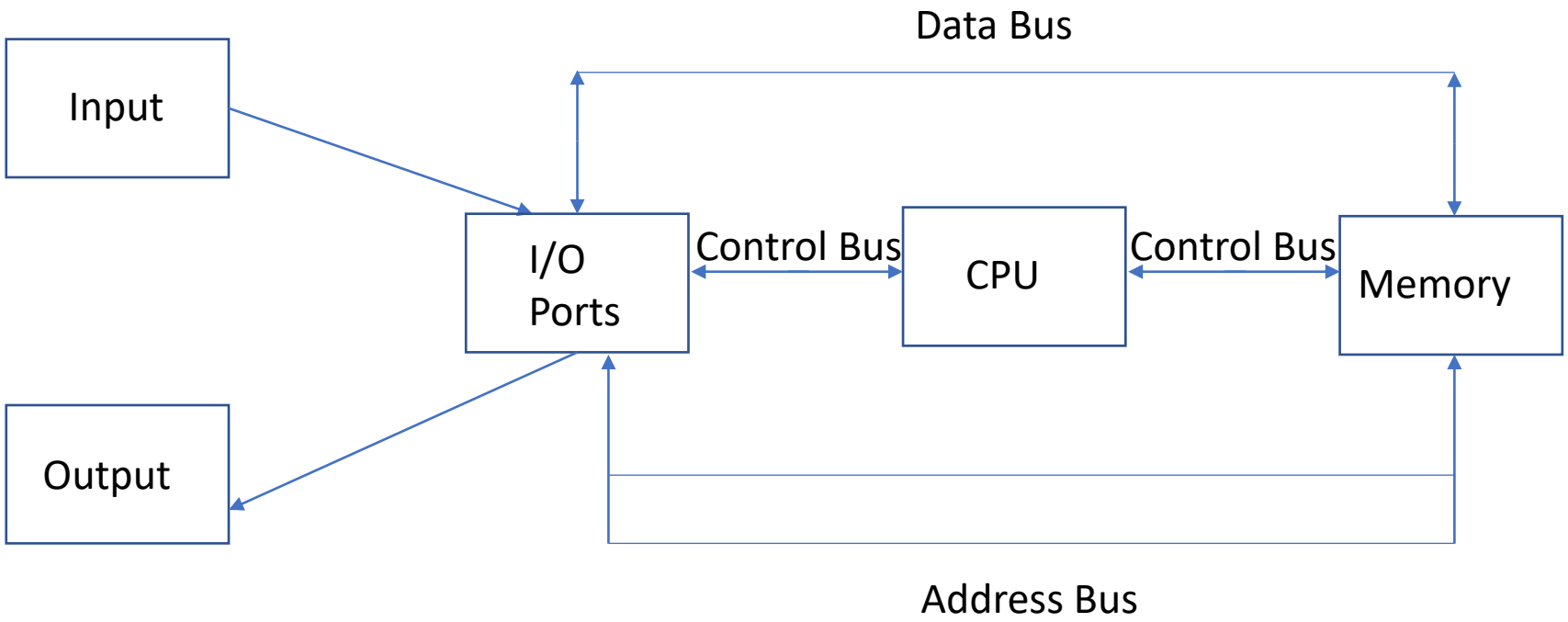

Figure (1)
Microcomputer

8086 Microprocessor

- The main characteristics of 8086 microprocessor are:-
- It has 16-bits registers.
- It has 20 address lines.
- It has 16 data lines.
- It consists powerful instruction sets, which provide operations like multiplication and division easily.
- It supports two modes of operation, minimum and maximum mode.
- Maximum mode is suitable for system having multiple processors and minimum mode is suitable for system having a single processor.
- It has pipeline architecture.

- Figure -2- illustrates pin-outs of 8086 & 8088.
  - –both are packaged in 40-pin **dual in-line** packages (DIPs)
- 8086 is a 16-bit microprocessor with a 16-bit data bus; 8088 has an 8-bit data bus.
  - –8086 has pin connections AD0–AD15
  - –8088 has pin connections AD0–AD7
- Data bus width is the only major difference.
  - thus 8086 transfers 16-bit data more efficiently

The pin-out of the 8086 in maximum mode; (b) the pin-out of the 8086 in minimum mode.

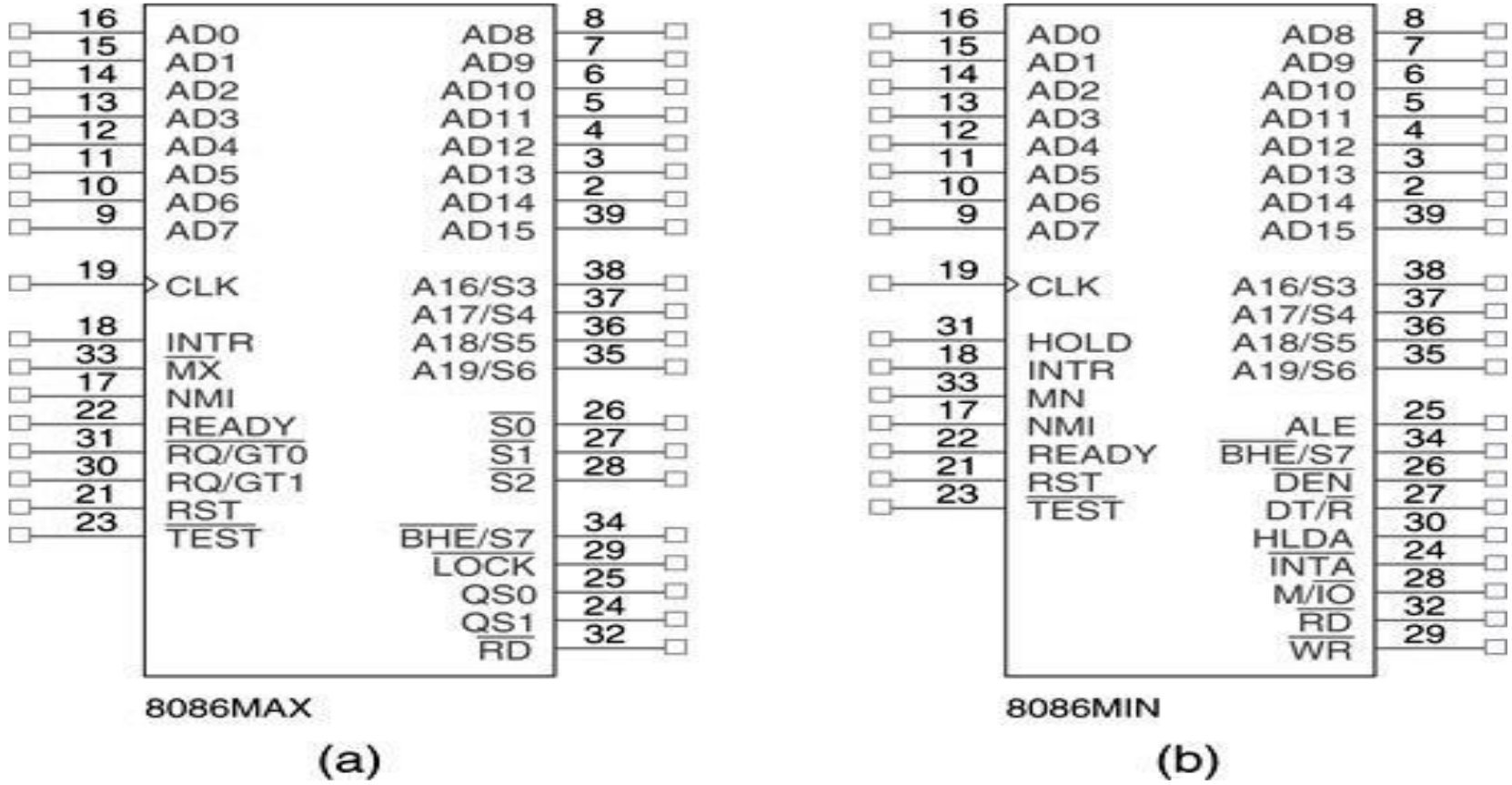

Figure (2)

8088 MP

Pin Connections AD7 - AD0

- 8088 **address/data bus** lines are multiplexed
  - –and contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1)
  - –or data whenever ALE is inactive (logic 0)
  - – ALE means address latch enable
- These pins are at their high-impedance state during a hold acknowledge.

Pin Connections A15 - A8

- 8088 **address bus** provides the upper-half memory address bits that are present throughout a bus cycle.
- These address connections go to their high-impedance state during a hold acknowledge.

8086 MP

- 8086 **address/data bus** lines compose upper multiplexed address/data bus on the 8086.
- These lines contain address bits A15–A8 whenever ALE is a logic 1, and data bus connections D15–D8 when ALE is a logic 0.
- These pins enter a high-impedance state when a hold acknowledge occurs.

Pin Connections A19/S6 - A16/S3

- **Address/status bus** bits are multiplexed to provide address signals A19–A16 and status bits S6–S3.

  –high-impedance state during hold acknowledge

  –status bit S6 is always logic 0,

  –bit S5 indicates the condition of the IF flag bit

- S4 and S3 show which segment is accessed during the current bus cycle.

  –these status bits can address four separate 1M byte memory banks by decoding as A21 and A20

- 8086 MP features

1. It is 16-bit microprocessor

2. It has a 16-bit data bus, so it can read data from or write data to memory and ports either 16-bit or 8-bit at a time.

3. It has 20 bits address bus and can access up to to (1 MB).

4. It can support up to 64K I/O ports.

5. It provides 14, 16-bit registers .

6. It has multiplexed address and data bus AD0-AD15 & A16-A19

7. It requires single phase clock with 33% duty cycle to provide internal timing.

8. Prefetches up to 6 instruction bytes from memory and queues them in order to speed up the processing.

9. 8086 supports 2 modes of operation a. Minimum mode b. Maximum mode

Pin Connections VCC

- This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.

GND

- The **ground** connection is the return for the power supply.
  - –8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation

BHE S7

- The **bus high enable** pin is used in 8086 to enable the most-significant data bus bits (D15–D8) during a read or a write operation.
- The state of S7 is always a logic 1.

Minimum Mode Pins $\overline{\boldsymbol{WR}}$

- **Write line** indicates 8086/8088 is outputting data to a memory or I/O device.
  - –during the time $\overline{\boldsymbol{WR}}$ is a logic 0, the data bus contains valid data for memory or I/O.
  - –high-impedance during a hold acknowledge.

Pin Connections $\overline{RD}$

- When **read signal** is logic 0, the data bus is receptive to data from memory or I/O devices

  –pin floats high-impedance state during a hold acknowledge

Ready

- Inserts wait states into the timing.

  –if placed at a logic 0, the microprocessor enters into wait states and remains idle

  –if logic 1, no effect on the operation

  _ Ready causes wait states for slower memory or I/O devices.

Minimum Mode Pins **DEN**

- **Data bus enable** activates external data bus buffers.

HOLD

- **Hold input** requests a direct memory access (DMA).
  - –if HOLD signal is a logic 1, the microprocessor stops executing software and places address, data, and control bus at high-impedance
  - –if a logic 0, software executes normally.

HLDA (Hold Acknowledge)

Indicates that the microprocessor has entered the hold state.

Minimum Mode Pins

- Minimum mode operation is obtained by connecting the $MN/\overline{MX}$ pin directly to +5.0 V.
  - –do not connect to +5.0 V through a pull-up register; it will not function correctly

$IO/\overline{M}$ or $M/\overline{IO}$

- The $IO/\overline{M}$ (8088) or $M/\overline{IO}$ (8086) pin selects memory or I/O.
  - –indicates the address bus contains either a memory address or an I/O port address.
  - –high-impedance state during hold acknowledge

***Minimum Mode Pins* ALE**

•**Address latch enable** shows the 8086/8088 address/data bus contains an address.

–can be a memory address or an I/O port number

–ALE signal doesn't float during hold acknowledge

$\boldsymbol{DT/\overline{R}}$

•The **data transmit/receive** signal shows that the microprocessor data bus is transmitting ($\boldsymbol{DT/\overline{R}}$) or receiving ($\boldsymbol{DT/\overline{R}}$ **= 0**) data.

–used to enable external data bus buffers .

$\boldsymbol{INTR}$

When $\boldsymbol{INTR}$**=1**, and IF =1, the microprocessor prepares to service interrupt.

$\overline{INTA}$

- The **interrupt acknowledge** signal is a response to the $INTR$ input pin.
  - –normally used to gate the interrupt vector number onto the data bus in response to an interrupt

$\boldsymbol{NMI}$

The non-maskable interrupt input is similar to $\boldsymbol{INT}$ **.**

-does not check the interrupt flag.

SS0

- The SS0 status line is equivalent to the S0 pin in maximum mode operation.
- Signal is combined with $IO/\overline{M}$ and $\boldsymbol{DT/\overline{R}}$ to decode the function of the current bus cycle.

BUS BUFFERING AND LATCHING

- Before 8086/8088 can be used with memory or I/O interfaces, their multiplexed buses must be demultiplexed.
- This section provides detail required to demultiplex the buses and illustrates how the buses are buffered for very large systems.
  - –because the maximum fan-out is 10, the system must be buffered if it contains more than 10 other components

Demultiplexing the 8088

- Figure (3) illustrates components required to demultiplex 8088 buses.

–two 74LS373 or 74LS573 transparent latches are used to demultiplex the address/data bus connections AD7–AD0

–and address/status connections A19/S6–A16/S3

- The latches, which are like wires whenever the address latch enable pin (ALE) becomes a logic 1, pass the inputs to the outputs.

8088 microprocessor shown with a demultiplexed address bus.

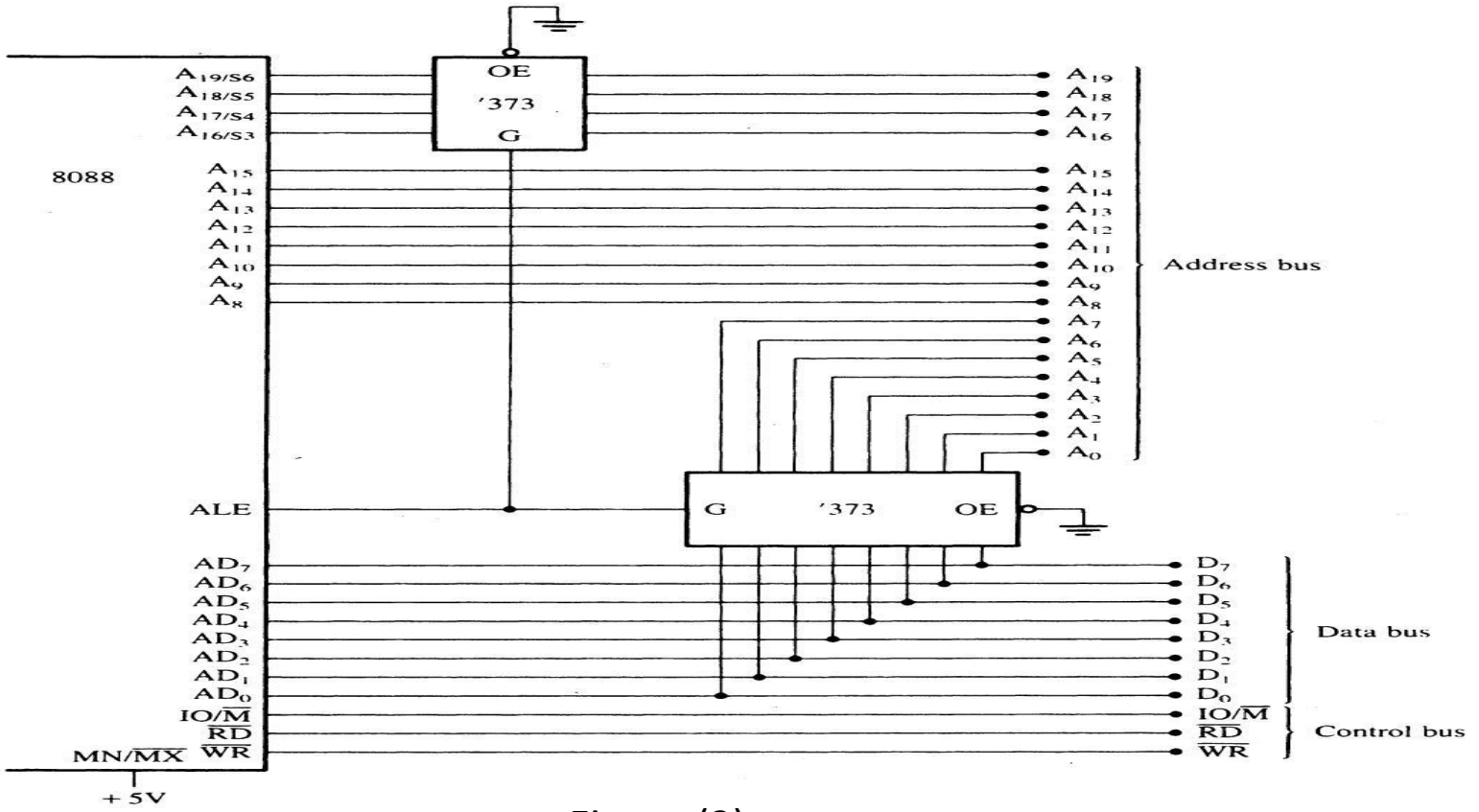

Figure (3)

- After a short time, ALE returns to logic 0 causing the latches to remember inputs at the time of the change to a logic 0.
- This yields a separate address bus with connections A19–A0.

  –these allow 8088 to address 1Mb of memory

- The separate data bus allows it to be connected to any 8-bit peripheral device or memory component.

- Fig (4) illustrates a demultiplexed 8086 with all three buses:
- address (A19–A0 and BHE)
- data (D15–D0),
- control ($M/\overline{IO}$,$\overline{RD}$, and $\overline{WR}$)
- Here, the memory and I/O system see the 8086 as a device with:

  -a 20-bit address bus;16-bit data bus

  -and a three-line control bus

The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems.

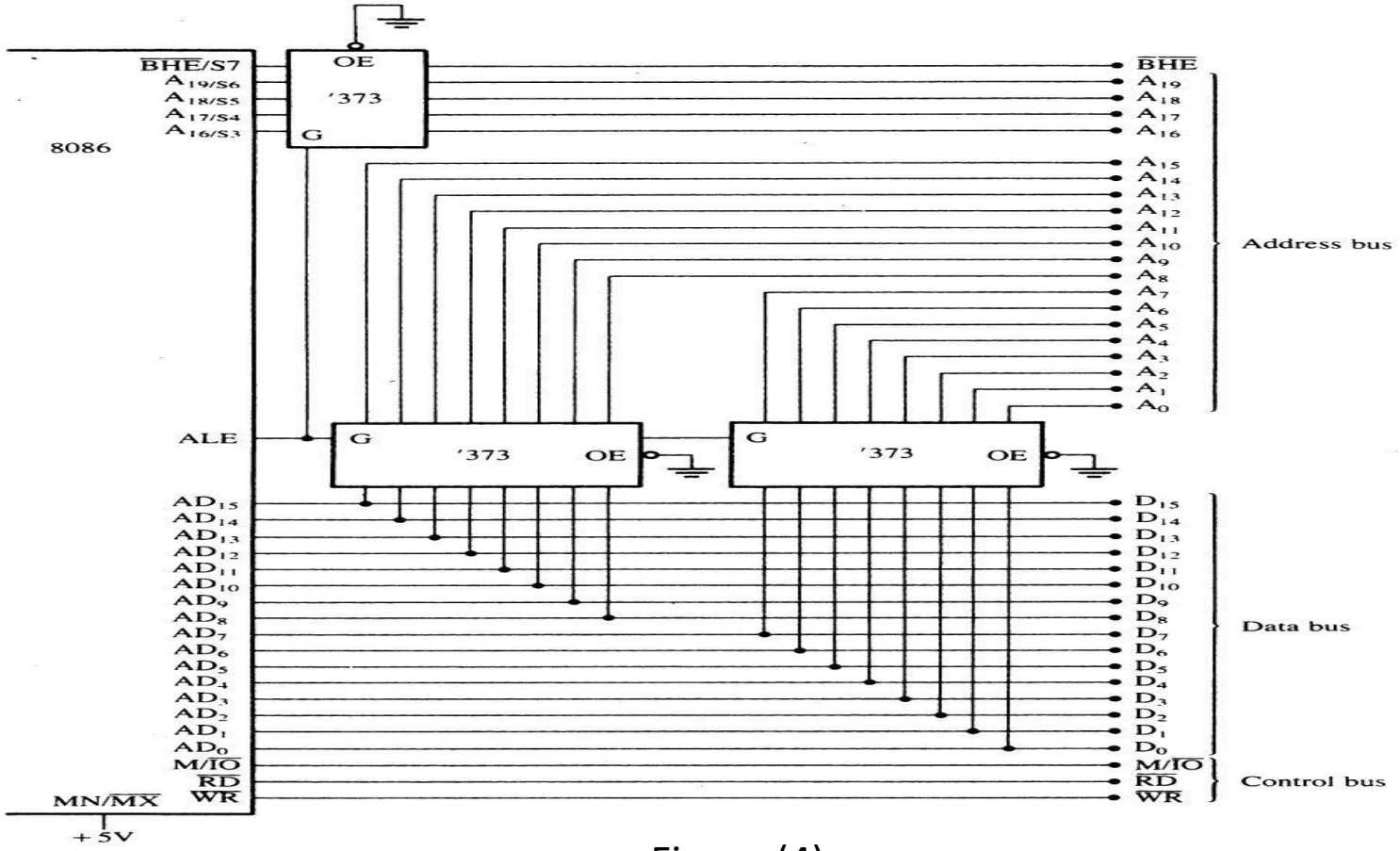

Figure (4)