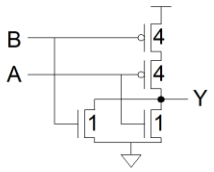
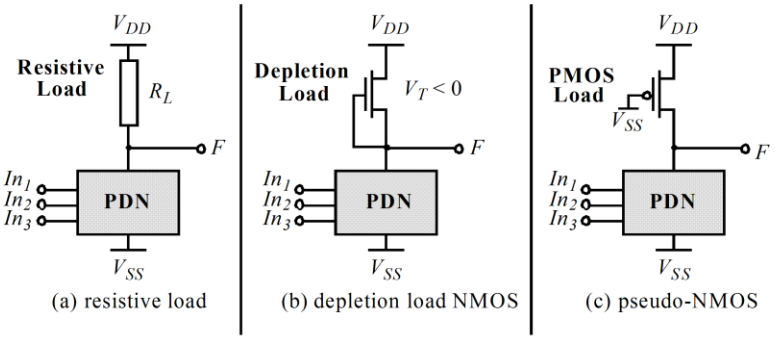
VLSI Circuits and Design Ratioed and Pass-Transistor Logic

Introduction

- What makes a circuit fast?
  - I = CdV/dt
    - dt = CdV/I
    - $\Delta t \propto (C/I)\Delta V$
  - fast circuit needs
    - low capacitance
    - high current
    - small swing
- PMOS are the enemy!
  - high capacitance for a given current
- Can we take the PMOS capacitance off the input?



Ratioed Logic



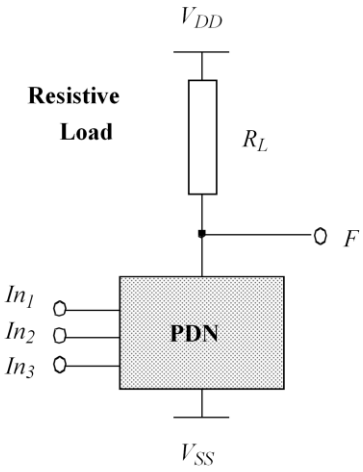
Goal: to reduce the number of devices over complementary CMOS

Ratioed, Pass Transistor Logic.3

The main concept of ratioed logic

1) Instead of using PUN and PDN (2N transistors), use ***a simple load device*** and PDN only.
2) The load device can be a passive or an active device.

Ratioed Logic



- **N transistors + Load**
- **$V_{OH} = V_{DD}$**
- $V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_L} V_{DD}$
- **Assymmetrical response ($t_r > t_f$)**
- **Static power consumption**
- **$t_{pLH} = 0.69 R_L C_L$**

Ratioed, Pass Transistor Logic.4

The over-simplified concept

- when the PDN is off, V_{OH} is pulled high by the load to strong logic '1'
- when the PDN is on, the V_{OL} will be determined by the voltage division
- $V_{OL} = (R_{PDN}/(R_{PDN}+R_L))V_{DD}$

To keep the N_{ML} high, $R_L >> R_{PDN}$. This is why it is called ratioed. The transistor must be carefully sized.

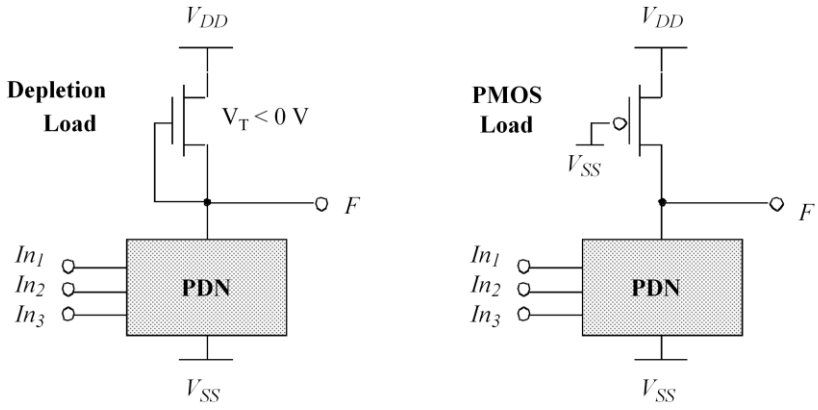
On the contrary, R_L must be small enough to allow fast switching

1) $t_{PLH} = 0.69 R_L C_L$
2) $t_{PHL} = 0.69(R_L || R_{PN}) C_L$

t_{PLH} is the main concern. $R_L >> R_{PDN}$ to maintain high noise margin, but small enough to enable fast switching.

Note also when the PDN is on, leakage current flows from V_{DD} to V_{SS} even in steady state.

Active Loads



Ratioed, Pass Transistor Logic.5

The left diagram shows the usage of depletion load NMOS as load device. Yes, all transistors are NMOS. Depletion mode NMOS has $V_T < 0$ V. This method was used during the NMOS era. The depletion NMOS is ON when $V_{GS} = 0$ V. In this case, the depletion load transistor is always on.

The second figure shows the pseudo-NMOS inverter. It resembles depletion load, but gives superior characteristics. Unlike the depletion transistor, the PMOS transistor does not have body effect since its source is always at V_{DD}, hence its V_{SB} is constant at 0 V.

The PMOS is driven by $V_{GSP} = -V_{DD}$ resulting in higher load current, compared to the other circuit, hence better rise time.

For pseudo-NMOS inverter, assuming V_{OL} is quite close to V_{SS} when $V_{in} = V_{DD}$, we make assumption that NMOS is linear and PMOS is velocity saturated. Equate currents

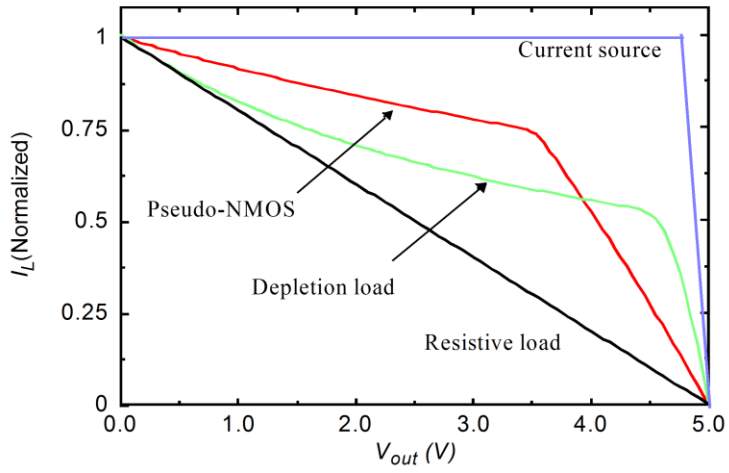
$$k_n\left((V_{DD}-V_{Tn})V_{OL}-\frac{V_{OL}^2}{2}\right)=|k_p|\left((V_{DD}-|V_{Tp}|)|V_{DSATp}|-\frac{V_{DSATp}^2}{2}\right)$$

Assuming $V_{DD} - V_{Tn} >> V_{OL}$, $V_{DD} - |V_{Tp}| >> V_{DSATp}$, and $V_{Tn} = |V_{Tp}|$

$$V_{OL}\approx\frac{|k_p|}{k_n}|V_{DSATp}|$$

Load Lines of Ratioed Gates

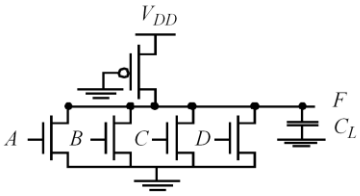
From Rabaey 1st ed.



Ratioed, Pass Transistor Logic.6

When using resistive load, $I_L = (V_{DD} - V_{OUT})/R_l$. The current drops as the output rises.

Pseudo-NMOS NOR Gate



$V_{OH} = V_{DD}$ *(similar to complementary CMOS)*

SMALLER AREA & LOAD BUT STATIC POWER DISSIPATION!

Ratioed, Pass Transistor Logic.7

Compared to complimentary CMOS, V_{OL} != 0 V due to ratioed nature of pseudo-NMOS structure.

All ratioed logic have these common attributes

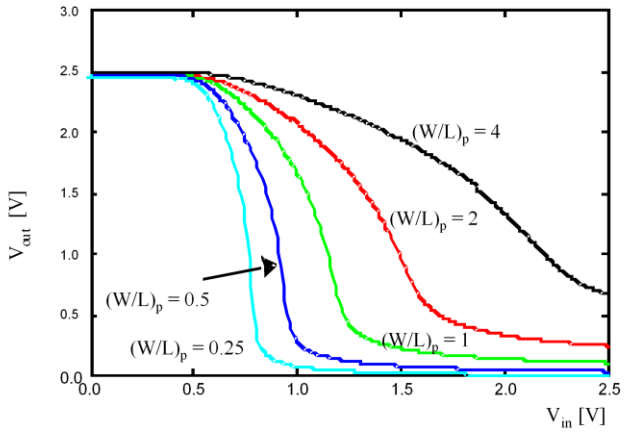
1) the VTC is assymmetrical

2) consumption of static power when output is low, due to direct current path between V_{DD} and V_{SS} through the load device

3) transistor scaling is very crucial

4) it uses only N+1 transistors instead of 2N for complimentary CMOS

Pseudo-NMOS VTC



Ratioed, Pass Transistor Logic.8

The VTC is for pseudo-NMOS inverter with NMOS size of 0.5 μm/0.25 μm. It demonstrates the effect of load transistor size on VTC.

From the curves, higher $(W/L)_p$ gives higher V_{OL} and higher static power consumption (and vice versa).

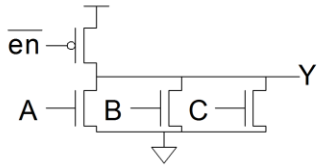
Exercise: Calculate V_{OL} using approx. eq. on p. 4 for case $(W/L)_p = 4$. Use transistor parameters on MOSFET transparency p. 22. Hint: Answer in text p. 266 is wrong!

Exercise: Repeat for case $(W/L)_p = 2$.

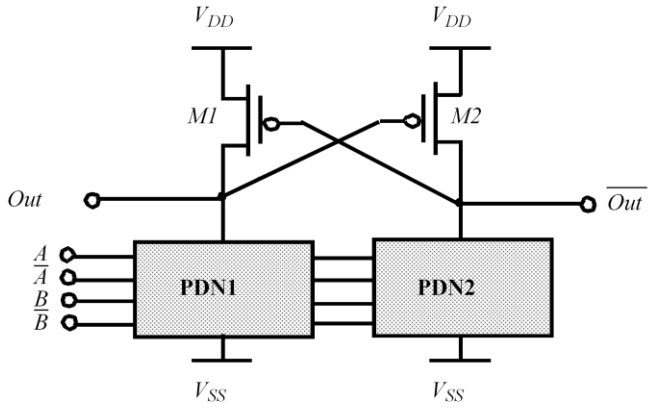
Exercise: Explain why answer is more accurate for 2nd case.

Pseudo-nMOS Power

- Pseudo-nMOS draws power whenever output is 0
  - static power
    - $P = I_{DD}V_{DD}$
  - A few µA/gate*1M gates would be a problem
- Use pseudo-nMOS sparingly for wide NORs
- Turn off pMOS when not in use

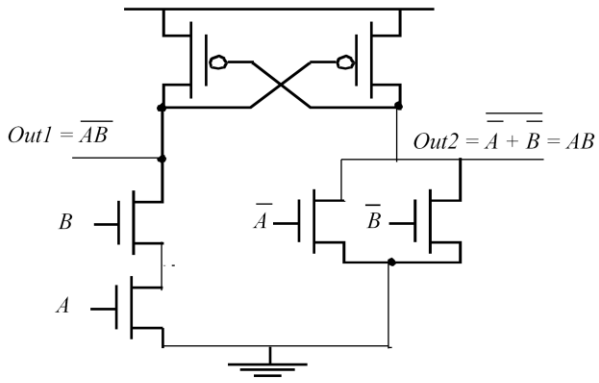


Improved Load



Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Example



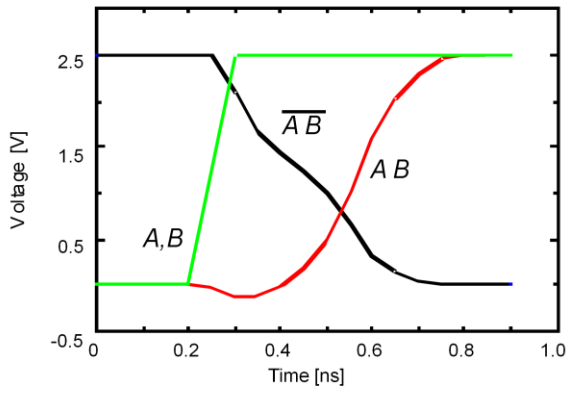
AND-NAND gate

If PDN1 is on, PDN2 is off, and vice versa.

Both outputs are at rail voltages (GND or V_{DD}). Steady state power dissipation is eliminated.

The circuit is still ratioed. Why? Say A = B = 0 V. Hence Out1 should be VDD and Out2 = GND. Thus left PMOS is on. When A = B = 1, Out1 should be LOW, which can be achieved by making sure the on resistance of PDN1 is low enough compared to on resistance of the left PMOS.

DCVSL Transient Response (AND-NAND gate)



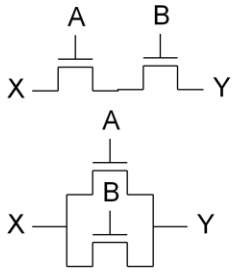
Ratioed, Pass Transistor Logic.12

Transistor dimensions used in the simulation

- A and B transistors: 1 μm/0.25 μm
- $\overline{A}$ and $\overline{B}$ transistors: 0.5 μm/0.25 μm
- PMOS transistors: 1.5 μm/0.25 μm

NMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



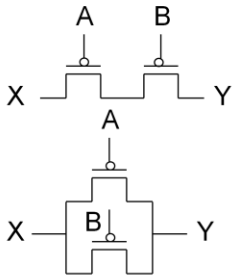
X = Y if A and B

X = Y if A or B

- Remember - NMOS transistors pass a strong 0 (output at 0 V) but a weak 1 (output at $V_{DD} - V_{Tn}$)

PMOS Transistors in Series/Parallel

- PMOS switch closes when the gate input is low

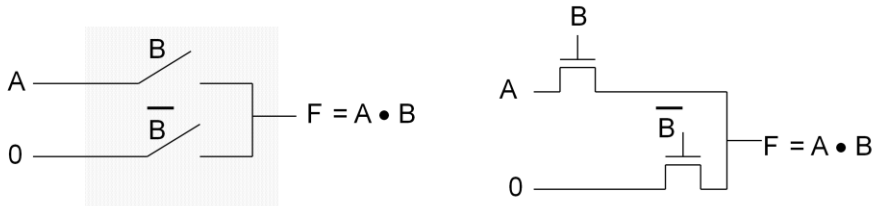


X = Y if $\overline{A}$ and $\overline{B}$

X = Y if $\overline{A}$ or $\overline{B}$

- Remember - PMOS transistors pass a strong 1 but a weak 0

Pass Transistor (PT) Logic



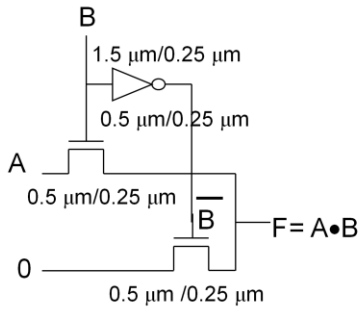
- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

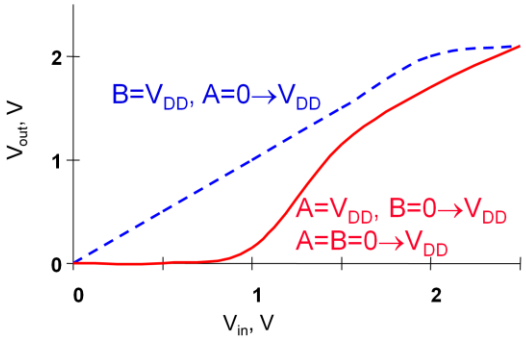
Ratioed, Pass Transistor Logic.15

This is pass transistor AND gate. How many transistors would it take to implement the same function in static comp. CMOS?

The switch driven by !B seems to be redundant. It is needed to ensure that a low impedance path exists to the supply rails under all circumstances. If the !B transistor is eliminated, what is the output when B is low?

VTC of PT AND Gate





- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can be fixed with static CMOS inverter insertion)

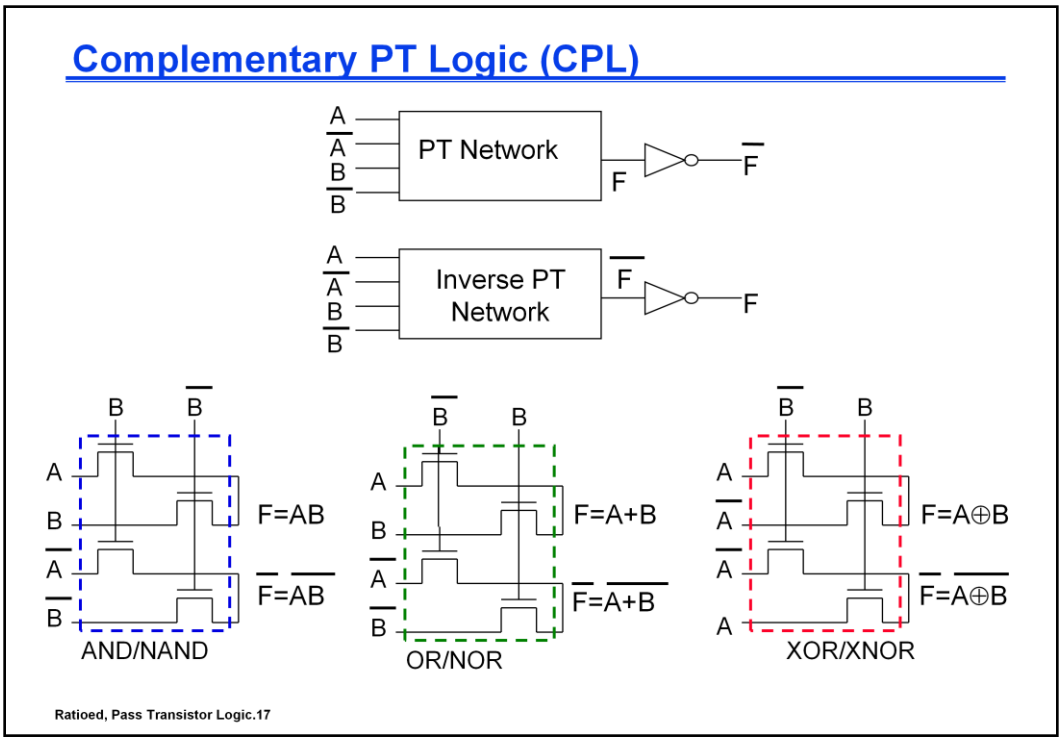
Ratioed, Pass Transistor Logic.16

VTC is data dependent.

For dotted line – Top pass transistor on, bottom off, input A rises from 0 → V_{DD}. Initially, V_{out} = A. When $V_{out} = V_{DD} - V_{Tn}$ (~ 2.1 V in this example), output stops rising although A increases. **Exercise: Explain why.**

For case where A = V_{DD} and B rises from 0 → V_{DD}, bottom transistor stays on (hence V_{out} is almost 0 V) until the inverter switches to zero (at ~ $V_{DD}/2$). V_{out} only rises once the bottom pass transistor turns off.

Observe that a pure PT gate is not REGENERATIVE. A gradual signal degradation will be observed after passing through a number of subsequent gates. Output degradation can be remedied by occasional insertion of a CMOS inverter.



How are the circuits built?

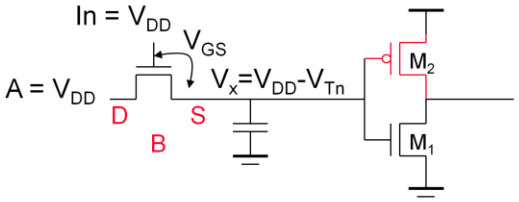
For NAND gate as an example, OUT = !(AB). We can rewrite OUT = !B + !A. We further rewrite OUT = !B!B + B!A. Hence transistor driven by !B is sourced by !B and transistor driven by B is sourced by !A.

For OR gate, OUT = A + B. We can rewrite OUT = (!B)A + B. We further rewrite OUT = (!B)A + BB. Hence transistor driven by !B is sourced by A and transistor driven by B is sourced by B.

CPL Properties

- CPL gates are differential circuits, hence complementary data inputs and outputs are always available
- Still static, since the output nodes are always tied to either V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead due to complementary signals

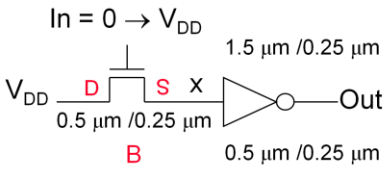
NMOS Only PT Driving an Inverter

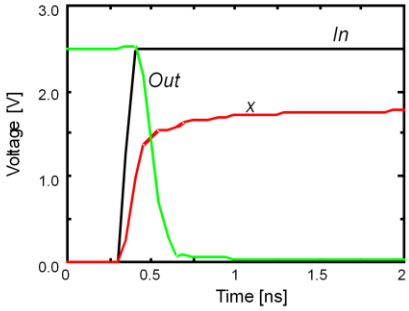


- V_x does not pull up to V_{DD}, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting, since its gate is not at V_{DD}, allowing current to flow from V_{DD} to GND via M_2 and M_1)
- V_{Tn} of PT increases because body effect (V_{SB} ~ V_{DD} for case above)

Body potential is at GND, hence $V_{SB} = V_S$.

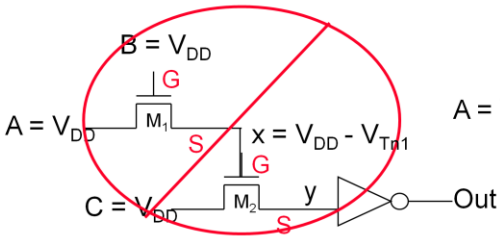
Voltage Swing of PT Driving an Inverter

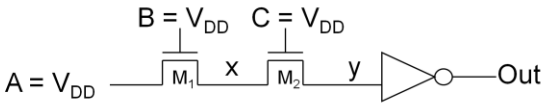




- Body effect due to large V_{SB}.
- From simulation result, Out ~ 1.8 V. Since Out = $V_{DD} - V_{Tn}$, we can deduce that V_{Tn} ~ 0.7 V (note: V_{Tn0} = 0.43 V).

Cascaded NMOS Only PTs





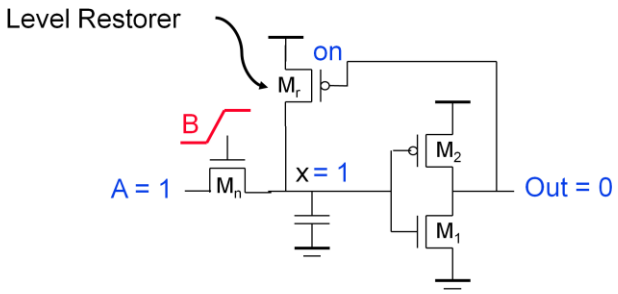
Swing on y = V_{DD} - V_{Tn1} - V_{Tn2}

Swing on y = V_{DD} - V_{Tn1}

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation (by inverter) and reduced noise margins

For circuit on the right, what is V_y if $V_C = V_{DD} – V_{Tn2}$?

Solution 1: Level Restorer



- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- For correct operation M_r must be sized correctly (ratioed)
- Restorer has speed and power impacts: increases the capacitance at x, slowing down the gate; increases t_r of Out (but decreases t_f)

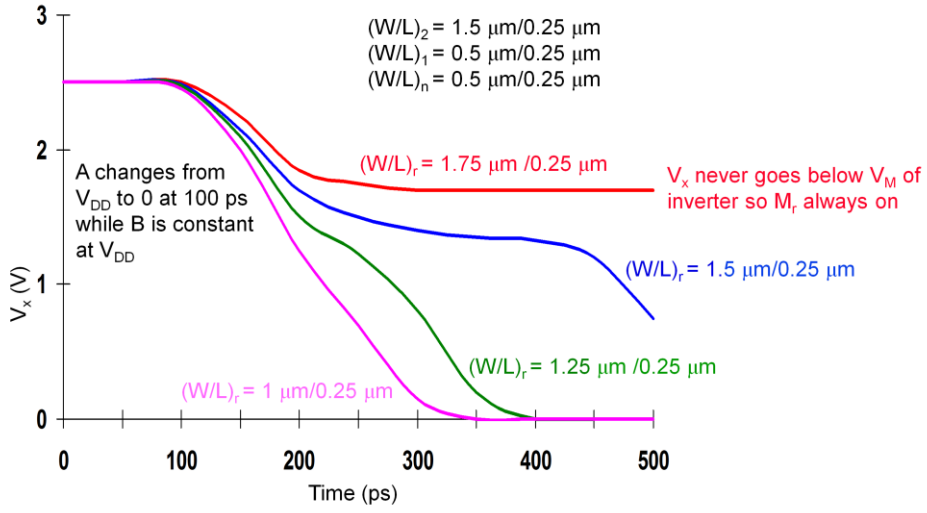
Ratioed, Pass Transistor Logic.22

Why ratioed?

When node x is 1 but logically should change to 0 (for e.g. when A changes to 0, while B remains 1), the pull-down network through M_n must be stronger than the pull-up network of M_r in order to switch node x to 0. If R_r is too small (i.e. W_r is too large), it is impossible to bring the voltage at node x below the switching threshold of the inverter.

Without M_r, x can be discharged easily. Out rise time is fast (assuming Out is initially low). With M_r present, it is on if Out is initially low. When x is to be discharged, M_n has to fight with the restorer. Hence x is discharged more slowly, which increases rise time of Out.

Transient Level Restorer Circuit Response

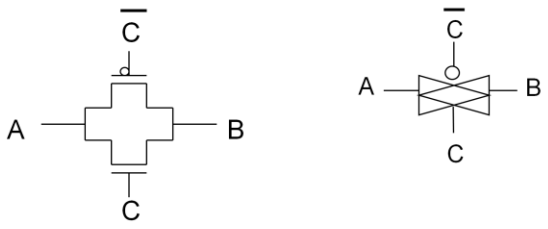


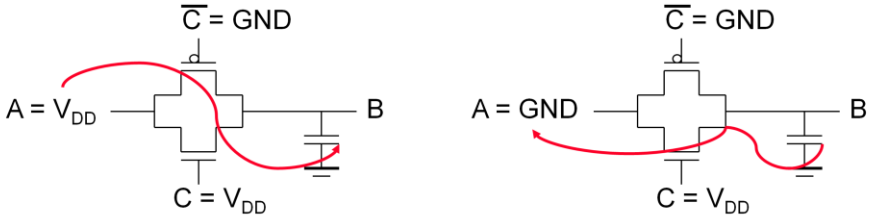
Ratioed, Pass Transistor Logic.23

Sizing of M_r is critical for DC functionality, not just performance!

Solution 2: Transmission Gates (TGs)

- Most widely used solution





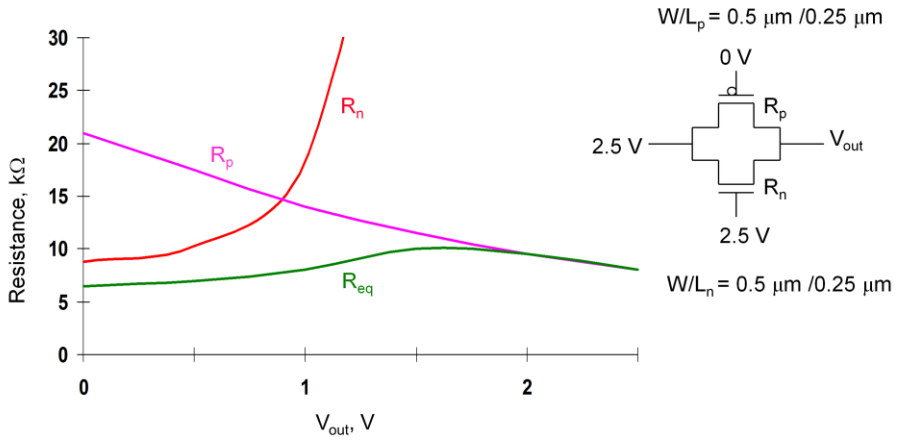
- Full swing *bidirectional* switch controlled by the gate signal C. A = B if C = 1. If C = 0, both transistors are off.

Use the NMOS to ensure both input and output terminals exactly equal to 0. Use the PMOS to ensure both terminals exactly at V_{DD}.

Use minimum size for both transistors. Increasing W/L has no net impact on switching delay (reduces resistance but increases diffusion capacitance).

Ratioless logic.

Resistance of TG



Ratioed, Pass Transistor Logic.25

Transmission gate is not an ideal switch – has series resistance.

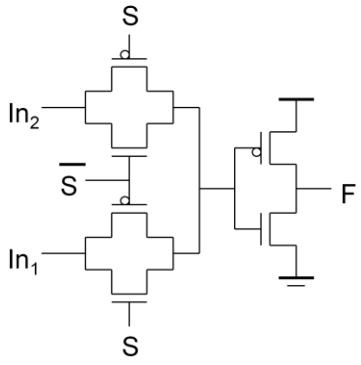
Effective resistance modeled as parallel connection of R_p and R_n ($R_p = (V_{DD} - V_{out})/I_p$).

For R_n, at low values of V_{out}, it is in saturation, hence has low resistance. As V_{out} increases, resistance increases to infinity (as device shuts off).

For R_p, at low values of V_{out}, it is in saturation. As V_{out} approaches V_{DD}, it operates in linear mode.

$R_{eq} = R_p \parallel R_n$ is relatively constant (about 8 kohms in this case).

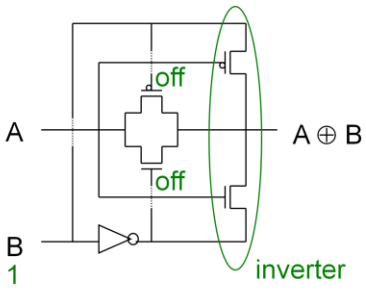
TG Multiplexer



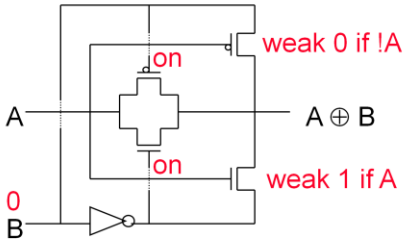
$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$

Complementary CMOS circuit has 8 transistors.

Transmission Gate XOR



output = !A when B = 1



When B = 0, output = A. TG guarantees perfect output whatever A is.

6 transistor implementation of XOR (versus 10 for complementary CMOS).

Output always has a connection to either VDD or GND.

Pass Transistor Summary

- Researchers investigated pass transistor logic for general purpose applications in the 1990's
  - benefits over static CMOS were small or negative
  - no longer generally used
- However, pass transistors still have niche in special circuits such as memories
  - they offer small size
  - threshold drops can be managed