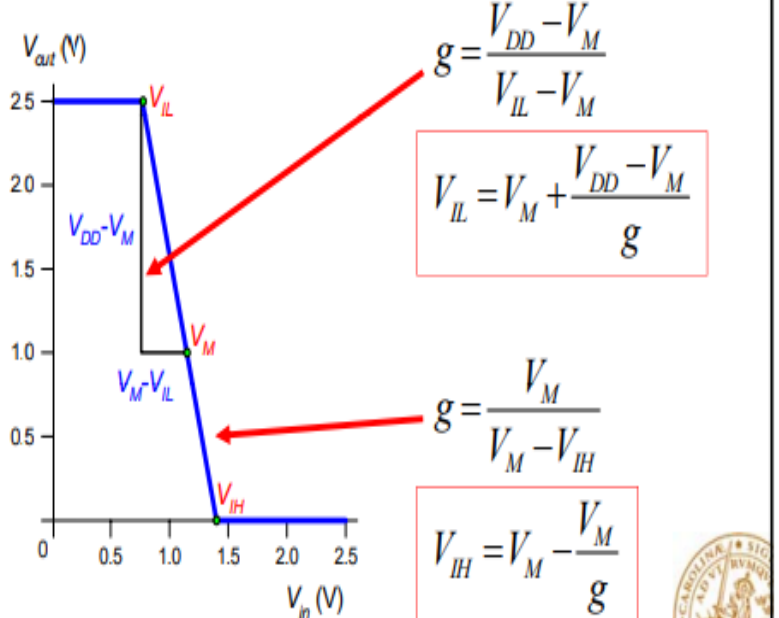
Lecture Six

Determining V_{IH} and V_{IL}

$$g = \frac{\Delta V_{OUT}}{\Delta V_{in}}$$



$$g = \frac{V_{DD} - V_M}{V_{IL} - V_M}$$

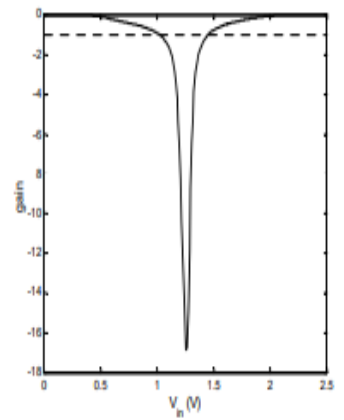
$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$g = \frac{V_M}{V_M - V_{IH}}$$

$$V_{IH} = V_M - \frac{V_M}{g}$$

The Inverter Gain (g)

$$g = -\frac{1}{I_D(V_M)} \frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \approx -\frac{1+r}{(V_M - V_{Tn} - \frac{V_{DSATn}}{2})(\lambda_n - \lambda_p)}$$



Note that the gain is very sensitive to the channel-length modulation

V_{IL} Maximum input voltage considered as logic ‘0’.

V_{IH} Minimum input voltage considered as logic ‘1’.

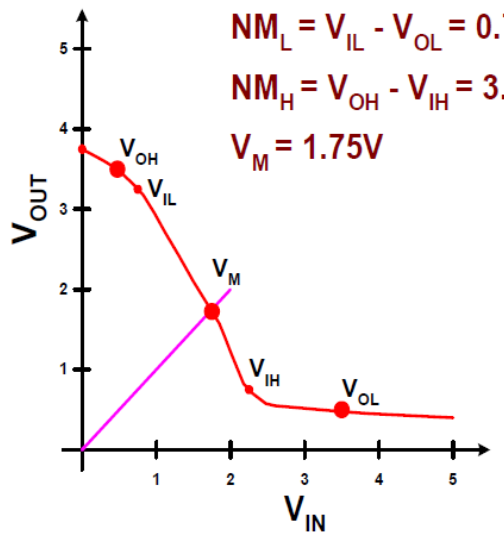
V_{OH} Minimum output voltage considered as logic ‘1’.

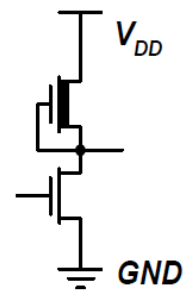
V_{OL} Maximum output voltage considered as logic ‘0’.

$NM_L = V_{IL} - V_{OL} = 0.75 - 0.50 = 0.25V$

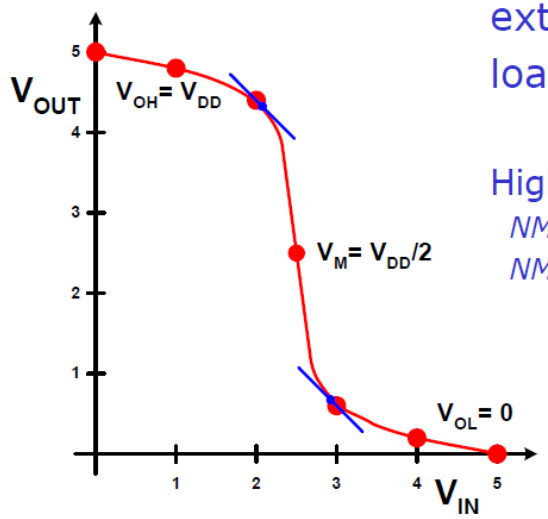
$NM_H = V_{OH} - V_{IH} = 3.50 - 2.25 = 1.25V$

$V_M = 1.75V$





CMOS Inverter VTC



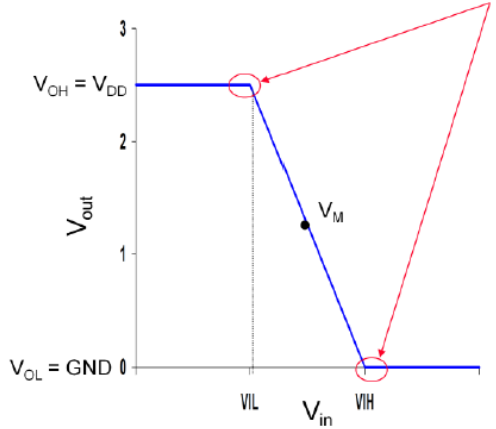
VTC graphically extracted from the load lines

High noise margin

$NM_H=V_{OH}-V_{IH} \approx 5-2.9 = 2.1V$

$NM_L=V_{IL}-V_{OL} \approx 2.1-0 = 2.1V$

Noise Margins: Determining V_{IH} and V_{IL}



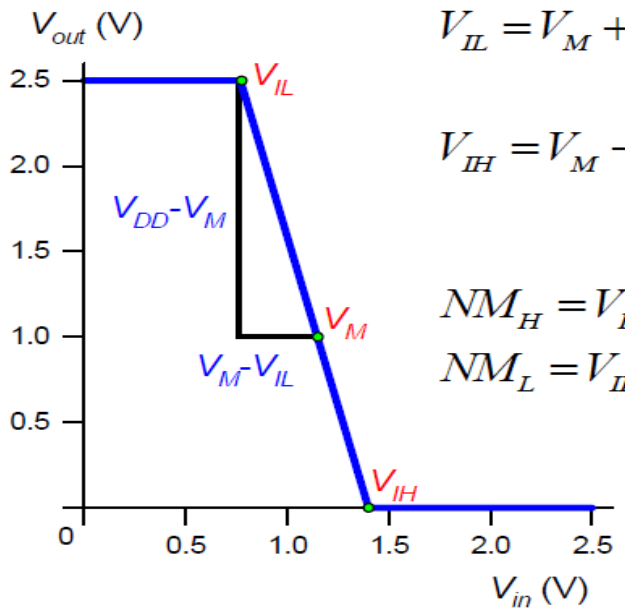
A piece-wise linear approximation of VTC

By definition, V_{IH} and V_{IL} are where $dV_{out}/dV_{in} = -1$ (= gain)

$NM_H = V_{DD} - V_{IH}$
$NM_L = V_{IL} - GND$

Approximating:
$V_{IH} = V_M - V_M/g$
$V_{IL} = V_M + (V_{DD} - V_M)/g$

High gain in the transition region is very desirable



$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} = 1 + \frac{2.5 - 1}{-34.6} = 0.96\ \text{V}$$

$$V_{IH} = V_M - \frac{V_M}{g} = 1 - \frac{1}{-34.6} = 1.03\ \text{V}$$

$$NM_H = V_{DD} - V_{IH} = 2.5 - 0.96 = 1.54\ \text{V}$$

$$NM_L = V_{IL} = 1.03\ \text{V}$$

Slightly to large values due to the approximation

Example:-

$Determine\ V_m$ if K_n=172.5,K_p=45, $V_{TN} = 0.43\ V, V_{TP} = -0.4, V_{DSATN}$ =0.63 V, V_{DSATP}=-1.0 V, V_{DD}=2.5 V ?

Solution:-

$$r = \frac{K_P V_{DSATP}}{K_N V_{DSATN}}$$

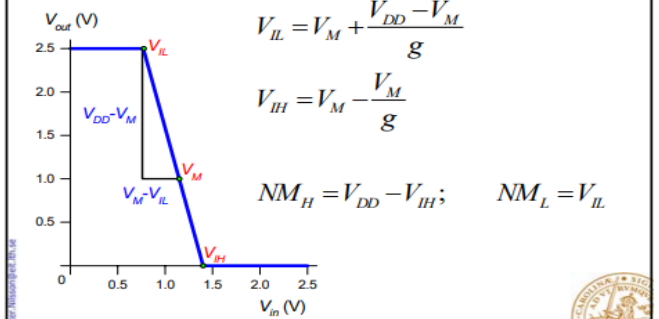
$$r = \frac{-45\times(-1)}{172.5\times0.63}=0.41$$

$$V_m=\frac{V_{TN}+\frac{V_{DSATN}}{2}+r\left(V_{DD}+V_{TP}+\frac{V_{DSATP}}{2}\right)}{1+r}$$

$$V_m = \frac{0.43 + \frac{0.63}{2} + 0.41\left(2.5 - 0.4 - \frac{1}{2}\right)}{1 + 0.41} = 1.0 \text{ V}$$

$$V_m \approx \frac{rV_{DD}}{1+r} = \frac{0.41 \times 1.5}{1 + 0.41} = 0.73 \text{ V}$$

Noise Margins

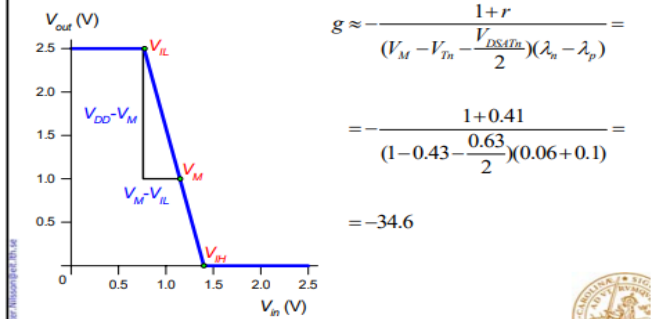


$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g}$$

$$NM_H = V_{DD} - V_{IH}; \qquad NM_L = V_{IL}$$

Example (Minimum sized transistors)



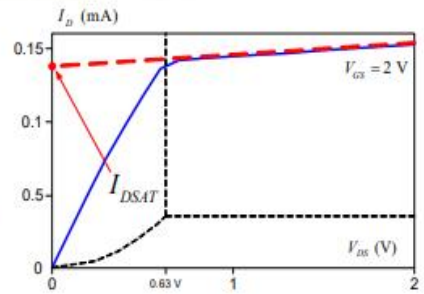
$$g \approx -\frac{1+r}{(V_M - V_{Tn} - \frac{V_{DSATn}}{2})(\lambda_n - \lambda_p)} =$$

$$= -\frac{1+0.41}{(1-0.43-\frac{0.63}{2})(0.06+0.1)} =$$

$$= -34.6$$

R_{eq} for Short Channel NMOS

Find I_{DSAT}



$V_{DD} = 2$ V; $V_T = 0.43$ V;

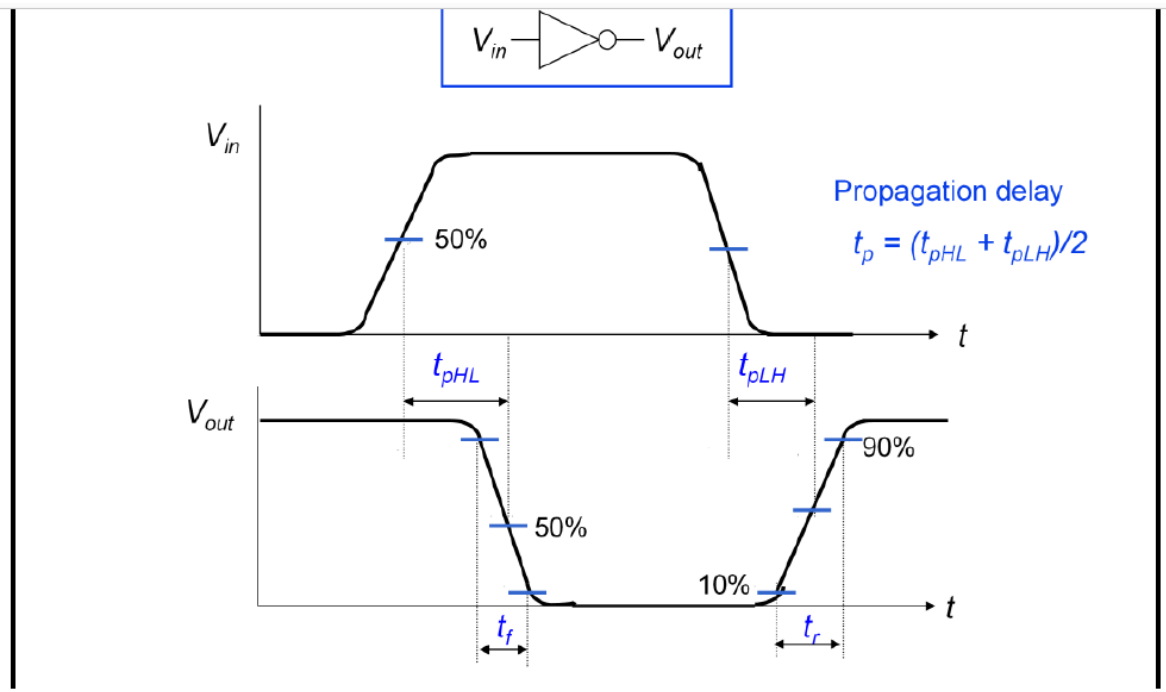
$V_{DSAT} = 0.63$ V; $k_n' = 115$ mA/V^2

$W = 0.375$ μm; $= 0.25$ μm

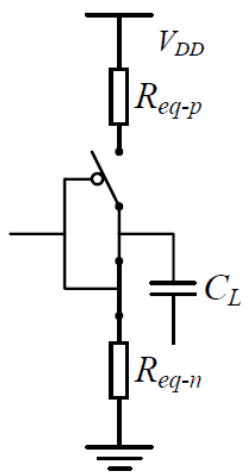
$I_{DSAT} = I_D$ when $V_{DS} = 0$ *(extrapolated)*

$$I_{DSAT} = k_n' \frac{W}{L}\left((V_{DD} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) =$$

$$I_{DSAT} = 115\frac{0.375}{0.25}\left((2-0.43)0.63 - \frac{0.63^2}{2}\right) = 136\ \mu\text{A}$$


V_{in}
V_{out}
V_{in}
50%
Propagation delay
$t_p = (t_{pHL} + t_{pLH})/2$
t
t_{pHL}
t_{pLH}
V_{out}
90%
50%
10%
t
t_f
t_r

Inverter - Transient Response

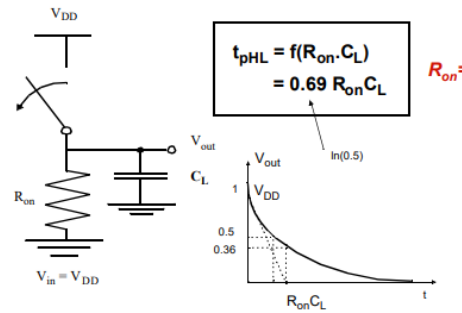


$C_L = 2\ fF; \qquad R_{eq-n} = 10\ k\Omega$

$t_r = 2.2RC = 2.2 \times 10 \times 10^3 \times 2 \times 10^{-15} = 44\ ps$

$t_{pHL} = 0.69RC = 0.69 \times 10 \times 10^3 \times 2 \times 10^{-15} = 14\ ps$

CMOS Inverter Propagation Delay



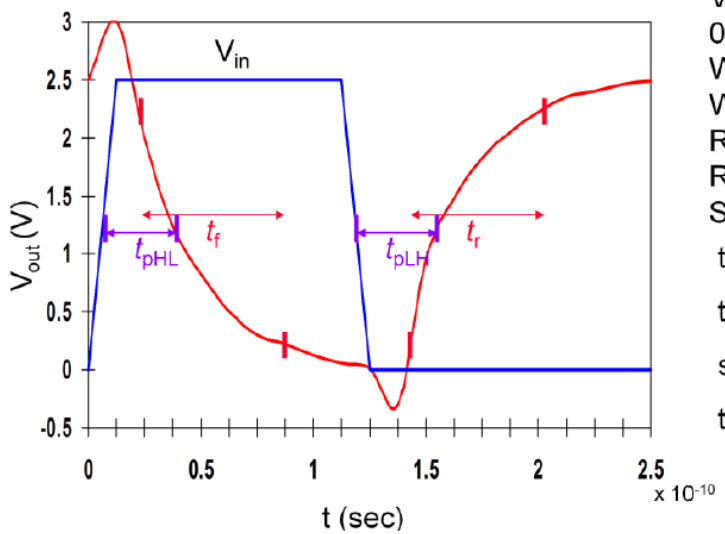
$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

$R_{on}=R_{eq}$

$$t_{pLH} = 0.69 R_{eqp} C_L$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

Inverter Transient Response



V_{DD}=2.5V
0.25µm
W/L_n = 1.5
W/L_p = 4.5
R_{eqn}= 13 kΩ (÷ 1.5)
R_{eqp}= 31 kΩ (÷ 4.5)
See p. 27 for C_L

t_{pHL} = 36 psec

t_{pLH} = 29 psec

so

t_p = 32.5 psec

C_{LLH} =6.fF

C_{LHL} =6.1fF

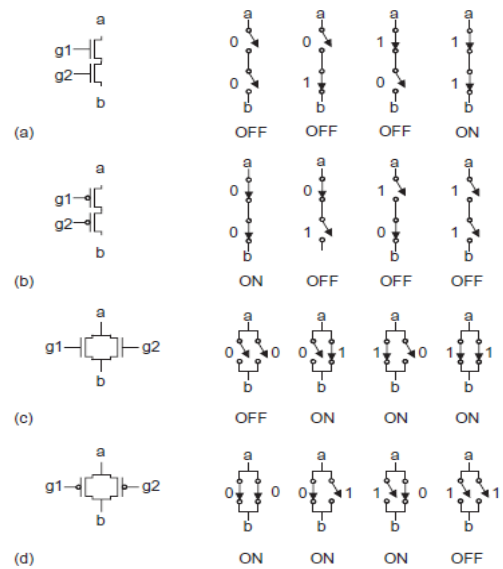
R_{eqn}=13 K$\boldsymbol{\Omega}$/1.5=8.67 K$\boldsymbol{\Omega}$

R_{eqp}=31 K$\boldsymbol{\Omega}$/4.5=8.89 K$\boldsymbol{\Omega}$

t_{pHL}=0.69× R_{eqn} × C_{LHL} =0.69 ×8.67 ×6.1=36ps

t_{pLH}=0.69× R_{eqp} × C_{LLH} =0.69 ×6.89 ×6.=29ps

$t_{p}=\frac{(t_{pHL}+t_{pLH})}{2}=\frac{36+29}{2}=32.5\ ps$

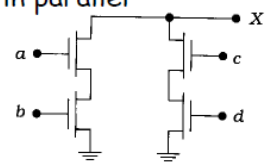


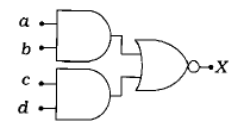
Connection and behavior of series and parallel transistors

AOI/OAI nMOS Circuits

- nMOS AOI structure
  - series txs in parallel

$F = \overline{a \cdot b + c \cdot d}$





- nMOS OAI structure
  - series of parallel txs

$F = \overline{(a + e) \cdot (b + f)}$