Lecture One

Very-large-scale integration (VLSI) is the process of creating an **integrated circuit** (IC) by combining thousands of **transistors** into a single chip. VLSI began in the 1970s when complex **semiconductor** and **communication** technologies were being developed. The **microprocessor** is a VLSI device.

Why VLSI?

Integration improves the design

Lower parasitic = higher speed

Lower power consumption

Physically smaller

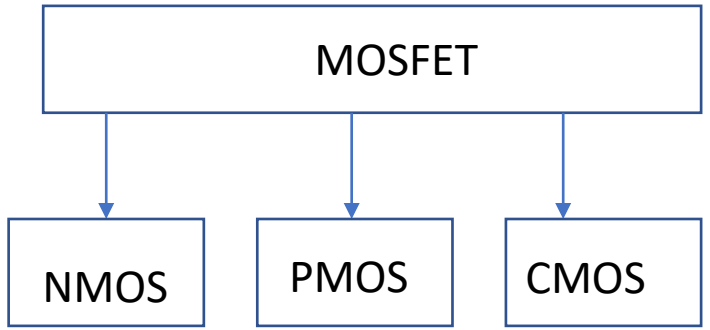
Integration reduces manufacturing cost –(almost)no manual assembly.

MOS (Metal oxide semiconductor)

Characteristics of MOS

- Fast
- Cheap
- Low Power Dissipation

Complementary :mixture of N-type and P-type leads to less power.

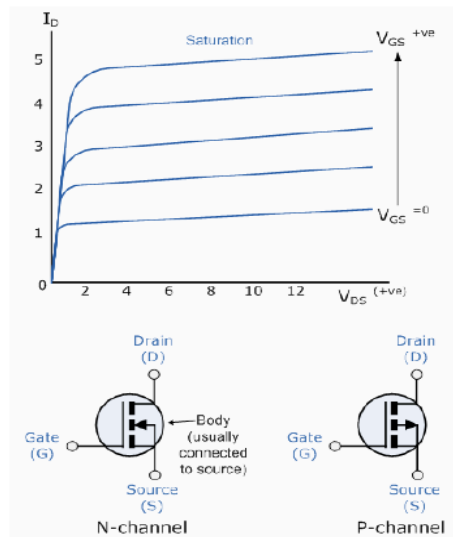

MOSFET
NMOS
PMOS
CMOS

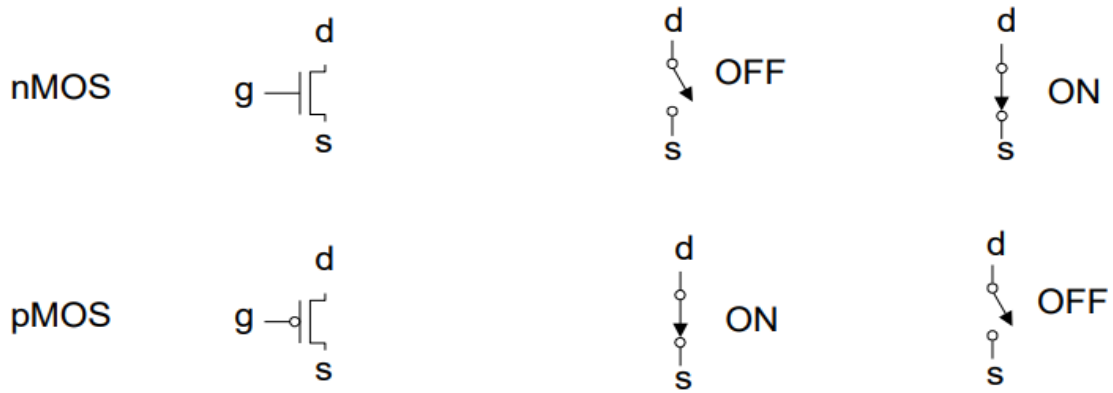
CMOS (complementary metal oxide semiconductor) Technology

- An Integrated circuit is an electronic network fabricated in a single piece of semiconductor material.
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns.
- The fabrication steps are sequenced to form three dimensional regions that act as transistors and interconnections that form the switching or amplification network.

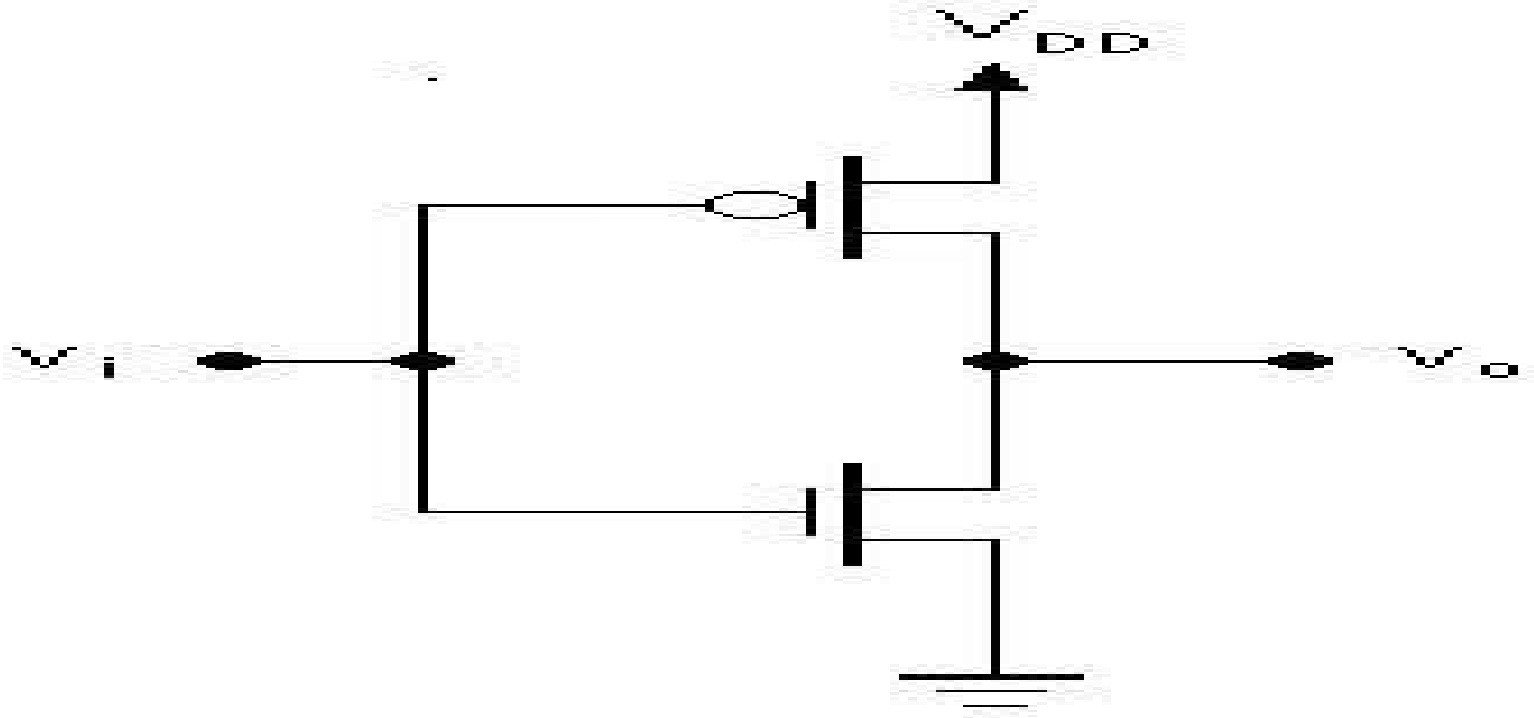
- NMOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority of carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

- P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate. The majority of carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.

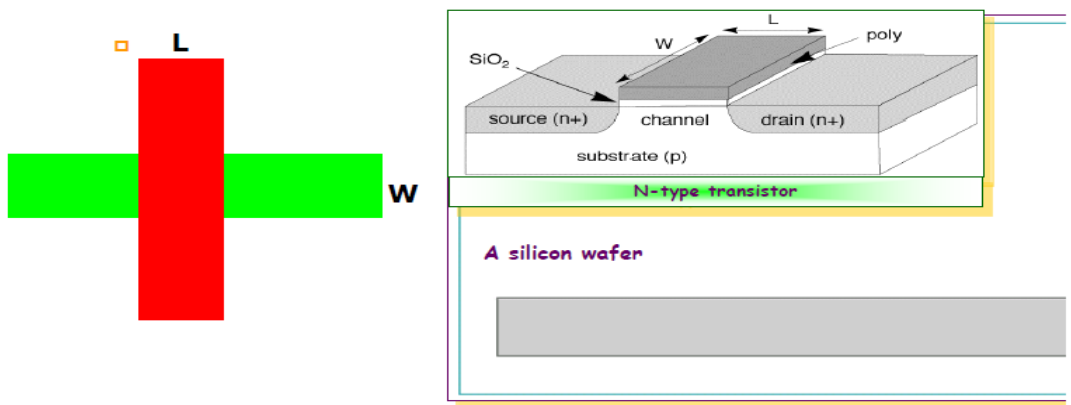

I_D
Saturation
V_{GS} +ve
5
4
3
2
1
0
V_{GS} =0
2
4
6
8
10
12
V_{DS} (+ve)
Drain (D)
Gate (G)
Body (usually connected to source)
Source (S)
N-channel
Drain (D)
Gate (G)
Source (S)
P-channel


nMOS
d
g
s
d
OFF
s
d
ON
s
pMOS
d
g
s
d
ON
s
d
OFF
s

CMOS –Invertor-



MOSFET


L
W
SiO2
W
L
poly
source (n+)
channel
drain (n+)
substrate (p)
N-type transistor
A silicon wafer

$\boldsymbol{\lambda}$ Based Design Rules:

- All device dimensions are expresses in terms of a scalable parameter $\boldsymbol{\lambda}$.
- $\boldsymbol{\lambda}$=L/2 ;L=The minimum feature size of transistor
- L=2 $\boldsymbol{\lambda}$
- These rules support proportional scaling.

NMOS Square law Model

$$I_G = 0$$

$$I_D = 0 \qquad \text{Cutoff}$$

$$= \frac{K_n W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{ohmic}$$

$K=\mu_n C_{ox}$
Conduction factor

$$= \frac{K_n W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad \text{saturation}$$

NMOS Square law Model- cont.

- Off region :
- $V_{GS} < V_T$

- Linear Region:
- $V_{GS} > V_T$, $0<V_{DS}<V_{GS}-V_T$

- Saturation Region:
- $V_{GS} > V_T$, $V_{DS}>V_{GS}-V_T$

- NMOS consists of n-type source and drain and a p-type substrate.
- In an NMOS, carriers are electrons When a high voltage is applied to the gate, the NMOS conducts If there is a low voltage at the gate, the NMOS will not conduct NMOS are said to be faster than PMOS because the charge carriers in NMOS, which are electrons, travel twice as fast as holes.
- NMOS ICs would be smaller than PMOS ICs NMOS can deliver half of the impedance delivered by a PMOS NMOS represents an N-type MOS transistor.

- PMOS is constructed with p-source and drain and an n-substrate.
- PMOS, carriers are holes. If a high voltage is applied to the gate, the PMOS will not conduct When a low voltage is applied to the gate,PMOS conducts Which are the carriers in PMOS.
- PMOS devices are less susceptible to interference than NMOS devices. PMOS represents a P-type MOS transistor.

CMOS:

- CMOS means complementary metal oxide semiconductor transistor.
- The CMOS circuit includes a PMOS transistor and an NMOS transistor.
- CMOS is more of a term from process technology.
- **Why do we use CMOS instead of PMOS and NMOS?**
- An advantage of CMOS over NMOS logic is that both low-high and high-low output transitions are fast since the on-state (PMOS) pull-up transistors are in contrast to the load resistors in NMOS logic have a low resistance. In addition, the output signal oscillates the full voltage between low and high rail.

The term CMOS stands for “Complementary Metal Oxide Semiconductor”. This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. Today’s computer memories, CPUs, and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs).

- **CMOS Working Principle**
- In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.
- In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

- Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.
- CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages (provided the source voltage is fixed).