Lecture Five

Case 1: V_{in}=0 V, V_{out}=5 V , V_{tn}=1 V, V_{tp}=-1 V Region A

NMOS $V_{GSN}= V_G - V_S = V_{in} - V_S$=0-0 =0 V

$\therefore V_{GSN} < V_{tn} \rightarrow$ CUT-OFF

PMOS $V_{GSP}= V_G - V_S = V_{in} - V_{DD}$=0-5 =-5 V

$\therefore V_{GSP} < V_{tP} \rightarrow$ -5 V $< -1V \rightarrow$ON (L/S)

$V_{DSP}= V_D - V_S = V_{OUT} - V_{DD}$=5V -5V =0 V

V_{GSP}- V_{tP}=-5 –(-1)=-4 V

$\therefore V_{DSP} > V_{GSP}$- $V_{tP} \rightarrow 0 > -4$ V $\rightarrow$ Linear

Case 2: V_{in}=1 V, V_{out}=5 V , V_{tn}=1 V, V_{tp}=-1 V Region B

NMOS $V_{GSN}= V_G - V_S = V_{in} - V_S$=1-0 =1 V

$\therefore V_{GSN}= V_{tn} \rightarrow$ ON (L/S)

$V_{DSN}= V_D - V_S= V_{out}- V_S$ =5-0=5V

$V_{DSN} > V_{GSN}- V_{tn} \rightarrow 5 > 1 - 1 \rightarrow 5 > 0 \rightarrow$ 0N $\rightarrow$ NMOS in saturation

PMOS $V_{GSP}= V_G - V_S = V_{in} - V_{DD}$=1-5 =-4 V

$\therefore V_{GSP} < V_{tP} \rightarrow$ON L/S

$V_{DSP}= V_D - V_S = V_{OUT} - V_{DD}$=5V -5V =0 V

$V_{DSP} > V_{GSP}- V_{tp} \rightarrow$0 >-4-(-1) $\rightarrow$0 >-3 $\rightarrow$Linear

Case 3: V_{in}=2.5 V, V_{out}=2.5 V , V_{tn}=1 V, V_{tp}=-1 V Region C

NMOS $V_{GSN}= V_G - V_S = V_{in} - V_S$=2.5-0 =2.5 V

$V_{GSN} > V_{tn} \rightarrow$ 2.5 V >1V $\rightarrow$ ON (L/S)

$V_{DSN}= V_D - V_S= V_{out}- V_S$ =2.5-0=2.5V

$V_{DSN} > V_{GSN} - V_{tn}$=2.5 V> 2.5V-1V $\rightarrow$ 2.5 V> 1.5V $\rightarrow$Saturation

PMOS $V_{GSP}= V_G - V_S = V_{in} - V_{DD}$=2.5-5 =-2.5 V

$V_{tp} > V_{GSP}$ $\rightarrow$-1V >-2.5V $\rightarrow$ON L/S

$V_{DSP}= V_D - V_S = V_{OUT} - V_{DD}$=2.5V -5V =-2.5 V

$V_{DSP} < V_{GSP}- V_{tp}$ $\rightarrow$-2.5V < -2.5-(-1) $\rightarrow$-2.5 < -1.5V $\rightarrow$Saturation

Case 4: V_{in}=4.0 V, V_{out}=1.0 V , V_{tn}=1 V, V_{tp}=-1 V Region D

NMOS V_{GSN}= $V_G - V_S$ = $V_{in} - V_S$=4.0-0 =4.0 V

$V_{GSN} > V_{tn} \rightarrow$ 4.5 V >1V → ON (L/S)

V_{DSN}= $V_D - V_S$= V_{out}- V_S =1.0-0=1.0V

$V_{DSN} < V_{GSN} - V_{tn}$ 1.0 V<3.V →Linear

PMOS V_{GSP}= $V_G - V_S$ = $V_{in} - V_{DD}$=4.-5. =-1.0 V → V_{GSP}= V_{tp} ON L/S

V_{DSP}= $V_D - V_S$ = $V_{OUT} - V_{DD}$=1.0V -5V =-4.0 V

$V_{DSP} <$ V_{GSP}- V_{tp} →-4.0V < -1.-(-1) →-4. < 0 V →Saturation

Case 5: V_{in}=5.0 V, V_{out}=0.0 V , V_{tn}=1 V, V_{tp}=-1 V Region E

NMOS V_{GSN}= $V_G - V_S$ = $V_{in} - V_S$=5.0-0 =5.0 V

$V_{GSN} > V_{tn} \rightarrow$ 5.0 V >1V $\rightarrow$ ON (L/S)

V_{DSN}= $V_D - V_S$= V_{out}- V_S =0.0-0=0.0V

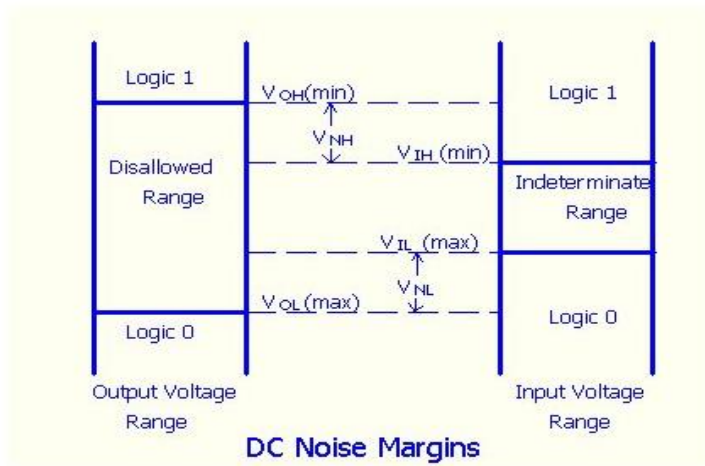
$V_{DSN} < V_{GSN} - V_{tn} \rightarrow$ 0.0 V<4.V $\rightarrow$Linear

PMOS V_{GSP}= $V_G - V_S$ = $V_{in} - V_{DD}$=5.-5. =0.0 V $\rightarrow V_{GSP} > V_{tp} \rightarrow$ OFF

CMOS INVERTER REGION OPERATIONS

REGION	CONDITION	PMOS	NMOS	OUTPUT
A	$0 \leq V_{in} \leq V_{tn}$	Linear	Cut-off	V_{out}=V_{DD}
B	$V_{tn} \leq V_{in} \leq V_{DD}/2$	Linear	Saturation	V_{out}=V_{DD}
C	$V_{in} = V_{DD}/2$	Saturation	Saturation	V_{out} sharps droply
D	$V_{DD/2} \leq V_{in} \leq V_{DD} - \lvert V_{tp} \rvert$	Saturation	Linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	Cut-off	Linear	V_{out}=0

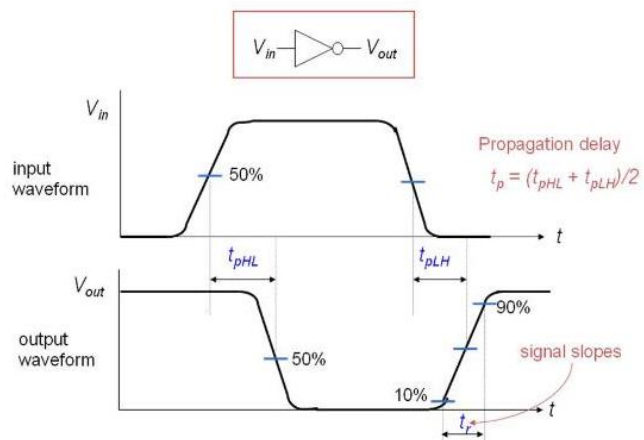
Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between on and off - but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts. The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching. The tolerance to noise can be measured by comparing the minimum input to the maximum output for each region of operation (on / off). This is more explicitly shown in the figure below.



Definition of noise margin

Noise margin : is a parameter intimately related to the transfer characteristics. It allows one to estimate the allowable noise voltage on the input of a gate so that the output will not be affected. Noise margin (also called noise immunity) is specified in terms of two parameters - the low noise margin N_L, and the high noise margin N_H . Referring to above figure, N_L is defined as the difference in magnitude between the maximum LOW input voltage recognized by the driven gate and the maximum LOW output voltage of the driving gate. That is, $N_L = |V_{IL} - V_{OL}|$. Similarly, the value of N_H is the difference in magnitude between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognizable by the driven gate. That is, $N_{MH} = |V_{OH} - V_{IH}|$. Where $V_{IH}|$: minimum HIGH input voltage, V_{IL}: maximum LOW input voltage, V_{OH}: minimum HIGH output voltage, V_{OL}: maximum LOW output voltage.

- **Inverter Dynamic Characteristics**
- Fig. below shows the dynamic characteristics of a CMOS inverter. The following are some formal definitions of temporal parameters of digital circuits. All percentages are of the steady state values.



Dynamic characteristics of CMOS inverter

- Rise Time (t_r) : Time taken to rise from 10% to 90%.
- Fall Time (t_f): Time taken to fall from 90% to 10%
- Edge Rate (t_{rf}): (t_r + t_f)/2.
- High-to-Low propagation delay (t_{pHL}): Time taken to fall from V_{OH} to 50%.
- Low-to-High propagation delay (t_{pLH}): Time taken to rise from 50% to V_{OL}.
- Propagation Delay (t_p): (t_{pHL} + t_{pLH})/2.
- Contamination Delay (t_{cd}): Minimum time from the input crossing 50% to the output crossing 50%