University of Diyala
College of engineering
Department of computer Engineering
Second class

microprocessor Programming

Lecture 1

8086 microprocessor

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Lecture 1
8086 microprocessor

- Over view
- Functional block
- Pins and Signals

Microprocessor

Unit II

8086 Microprocessor 8086

The Intel 8086 - architecture - MN/MX modes - 8086 addressing modes - instruction set- instruction format - assembler directives and operators - Programming with 8086 - interfacing memory and I/O ports - Comparison of 8086 and 8088 - Coprocessors - Intel 8087 - Familiarisation with Debug utility.

Program controlled semiconductor device (IC) which fetches (from memory), decodes and executes instructions.

It is used as CPU (Central Processing Unit) in computers.

First Generation
Between 1971 – 1973
PMOS technology, non compatible with TTL
4 bit processors ⇒ 16 pins
8 and 16 bit processors ⇒ 40 pins
Due to limitations of pins, signals are multiplexed

Second Generation
During 1973
NMOS technology ⇒ Faster speed, Higher density, Compatible with TTL
4 / 8/ 16 bit processors ⇒ 40 pins
Ability to address large memory spaces and I/O ports
Greater number of levels of subroutine nesting
Better interrupt handling capabilities

Intel 8085 (8 bit processor)

Third Generation
During 1978
HMOS technology ⇒ Faster speed, Higher packing density
16 bit processors ⇒ 40/ 48/ 64 pins
Easier to program
Dynamically relatable programs
Processor has multiply/ divide arithmetic hardware
More powerful interrupt handling capabilities
Flexible I/O port addressing

Intel 8086 (16 bit processor)

Fourth Generation
During 1980s
Low power version of HMOS technology (HCMOS)
32 bit processors
Physical memory space 2^{24} bytes = 16 Mb
Virtual memory space 2^{40} bytes = 1 Tb
Floating point hardware
Supports increased number of addressing modes

Intel 80386

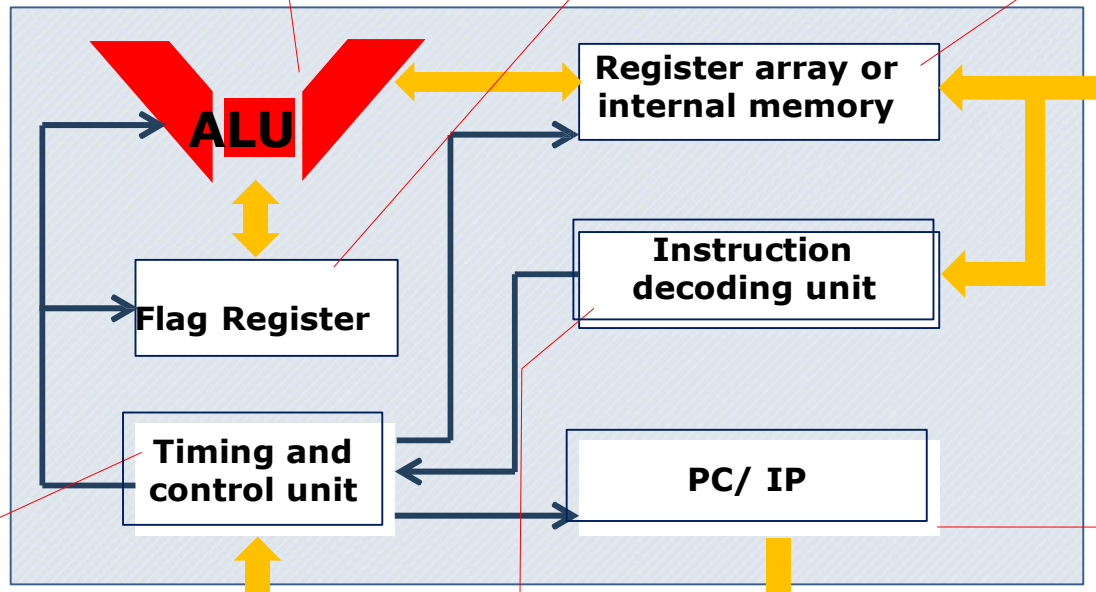
Fifth Generation **Pentium**

Functional blocks

Computational Unit; performs arithmetic and logic operations

Various conditions of the results are stored as status bits called flags in flag register

Internal storage of data



Generates the address of the instructions to be fetched from the memory and send Thorough address to the memoryto

Generationer l signals for internal and external operations sor of the microproces

Decodes instructions; sends information to the timing and control unit

Overview

- First 16- bit processor released by INTEL in the year 1978.
- Originally HMOS, now manufactured using HMOS III technique.
- Approximately 29, 000 transistors, 40 pin DIP, 5V supply.
- Does not have internal clock; external asymmetric clock source with 33% duty cycle.
- 20-bit address to access memory $\Rightarrow$ can address up to 2^{20} = 1 megabytes of memory space.
- Contains About 29000 Transistors.

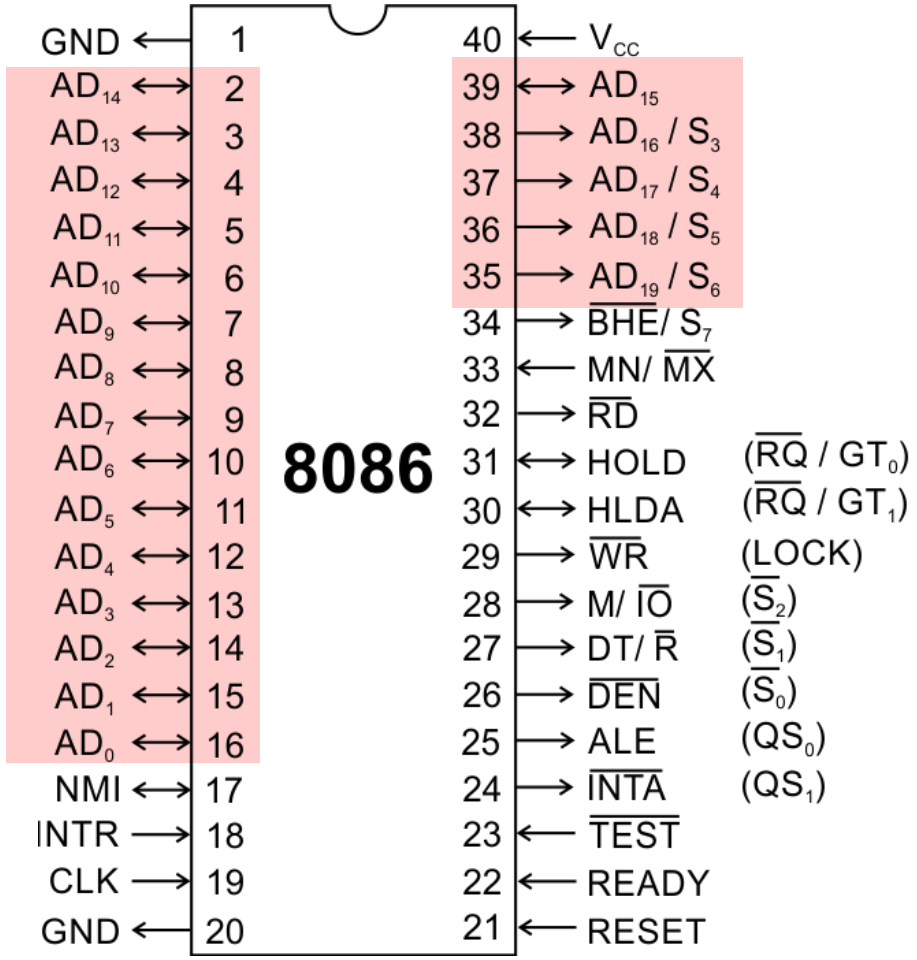
Addressable memory space is organized in to two banks of 512 kb each; Even (or lower) bank and Odd (or higher) bank. Address line A_0 is used to select even bank and control signal $\overline{BHE}$ is used to access odd bank

Uses a separate 16 bit address for I/O mapped devices $\Rightarrow$ can generate 2^{16} = 64 k addresses.

Operates in two modes: minimum mode and maximum mode, decided by the signal at MN and $\overline{MX}$ pins.

Pins and Signals

Common signals



AD_0-AD_{15} (Bidirectional)

Address/Data bus

Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A_0-A_{15}.

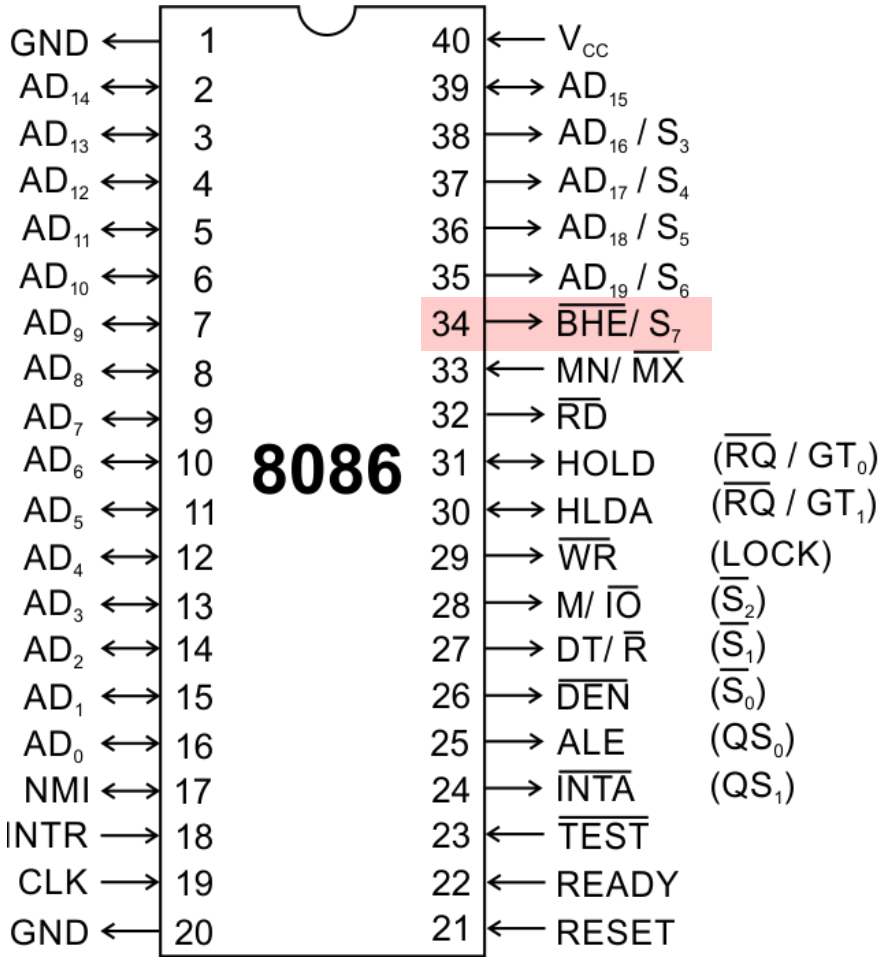
When data are transmitted over AD lines the symbol D is used in place of AD, for example D_0-D_7, D_8-D_{15} or D_0-D_{15}.

A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6

High order address bus. These are multiplexed with status signals

Pins and Signals

Common signals



BHE (Active Low)/S_7 (Output)

Bus High Enable/Status

It is used to enable data onto the most significant half of data bus, D_8-D_{15}. 8-bit device connected to upper half of the data bus use BHE (Active Low) signal. It is multiplexed with status signal S_7.

MN/ MX

MINIMUM / MAXIMUM

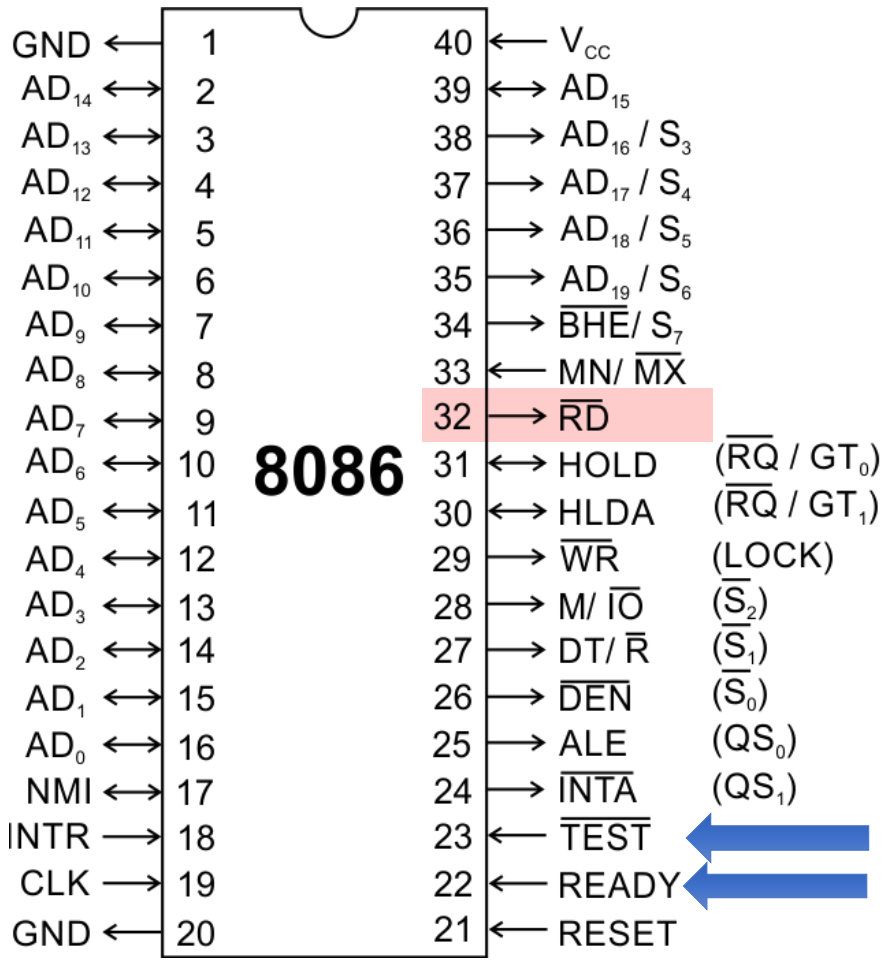
This pin signal indicates what mode the processor is to operate in.

RD (Read) (Active Low)

The signal is used for read operation. It is an output signal. It is active

Pins and Signals

Common signals



TEST

TEST input is tested by the 'WAIT' instruction.

8086 will enter a wait state after execution of the WAIT instruction and will resume execution only when the TEST is made low by an active hardware.

This is used to synchronize an external activity to the processor internal operation.

READY

This is the acknowledgement from the slow device or memory that they have completed the data transfer.

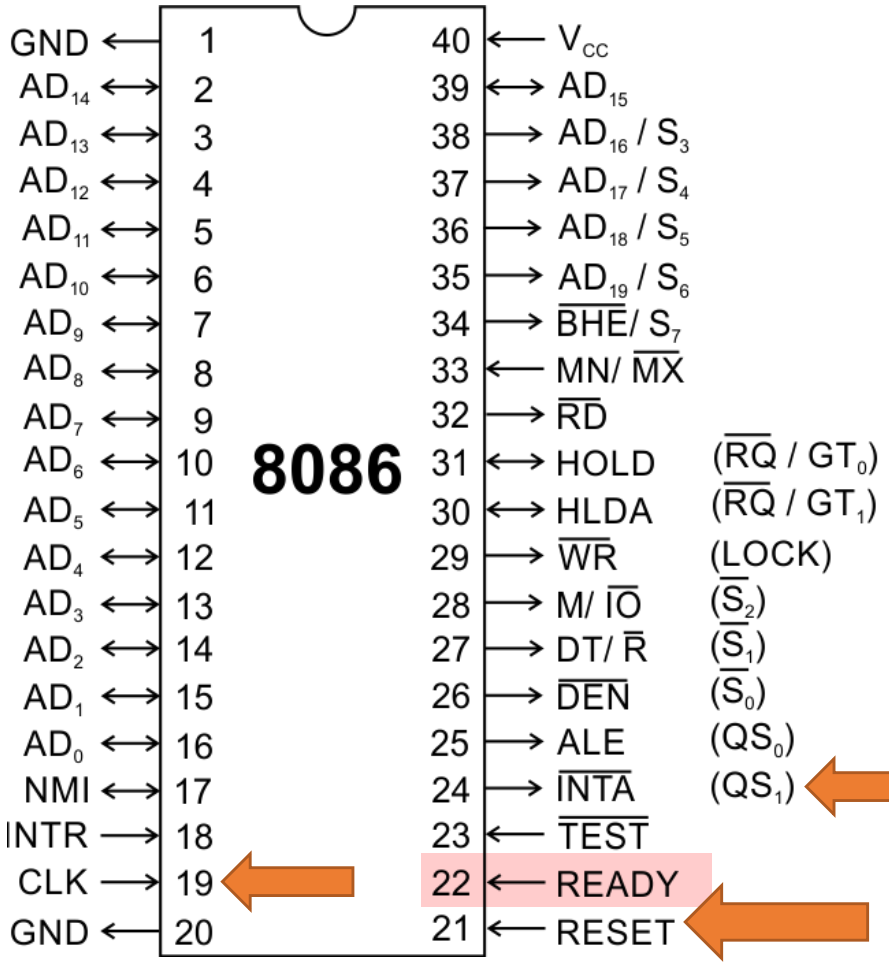
The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086.

The signal is active high.

8086 Microprocessor

Pins and Signals

Common signals



RESET (Input)

Causes the processor to immediately terminate its present activity.

The signal must be active HIGH for at least four clock cycles.

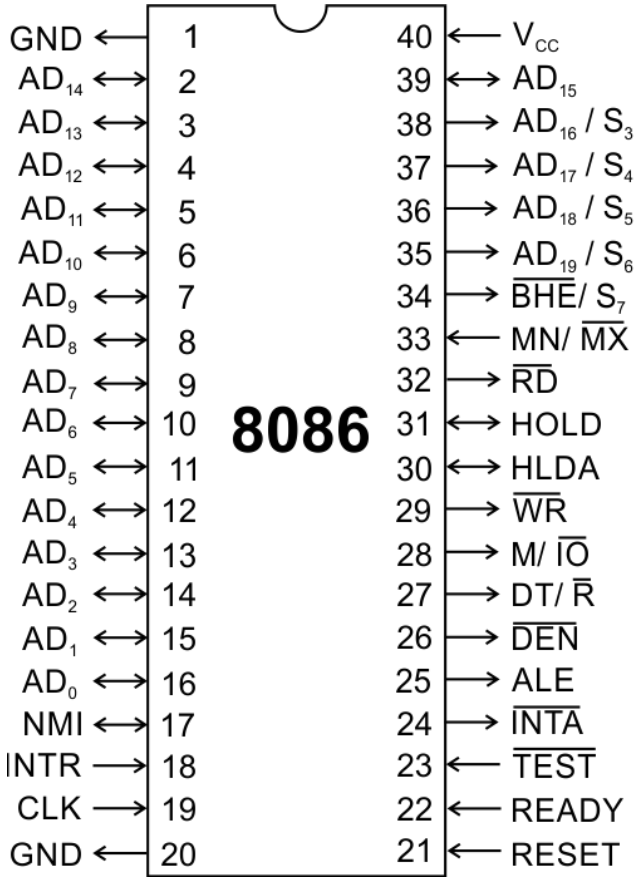
CLK

The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle.

INTR Interrupt Request

This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.

This signal is active high and internally synchronized.



The 8086 microprocessor can work in two modes of operations : Minimum mode and Maximum mode.

In the minimum mode of operation the 8086 Microprocessor do not associate with any co-processors and can not be used for multiprocessor systems.

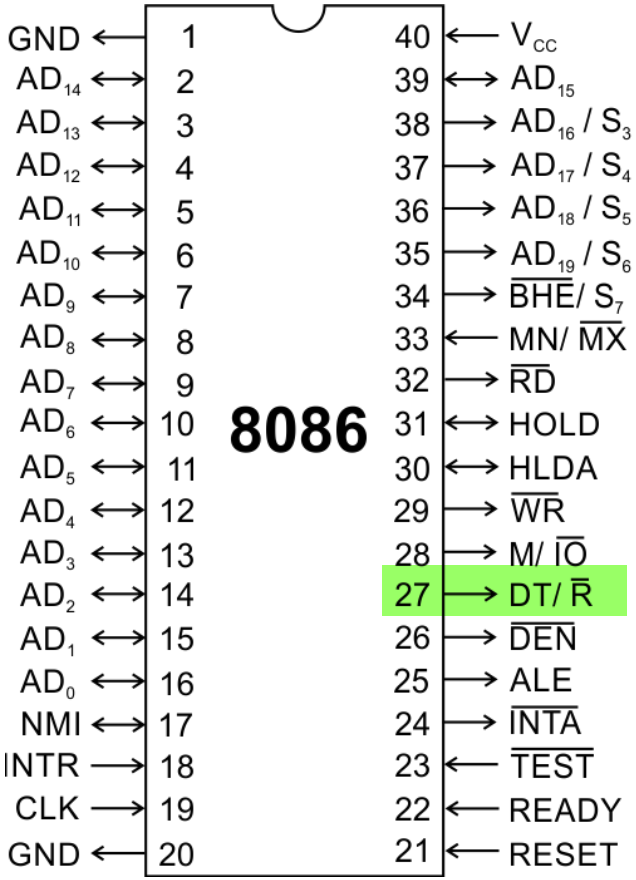
In the maximum mode the 8086 can work in multi-processor or co-processor configuration.

Minimum or maximum mode operations are decided by the pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.

Pins and Signals

Minimum mode signals



Pins 24 -31

For minimum mode operation, the MN/ $\overline{MX}$ is tied to VCC (logic high)

8086 itself generates all the bus control signals

DT/$\overline{R}$ — (Data Transmit/ Receive) Output signal from the processor to control the direction of data flow through the data transceivers

$\overline{DEN}$ — (Data Enable) Output signal from the processor used as out put enable for the transceivers

ALE — (Address Latch Enable) Used to demultiplex the address and data lines using external latches

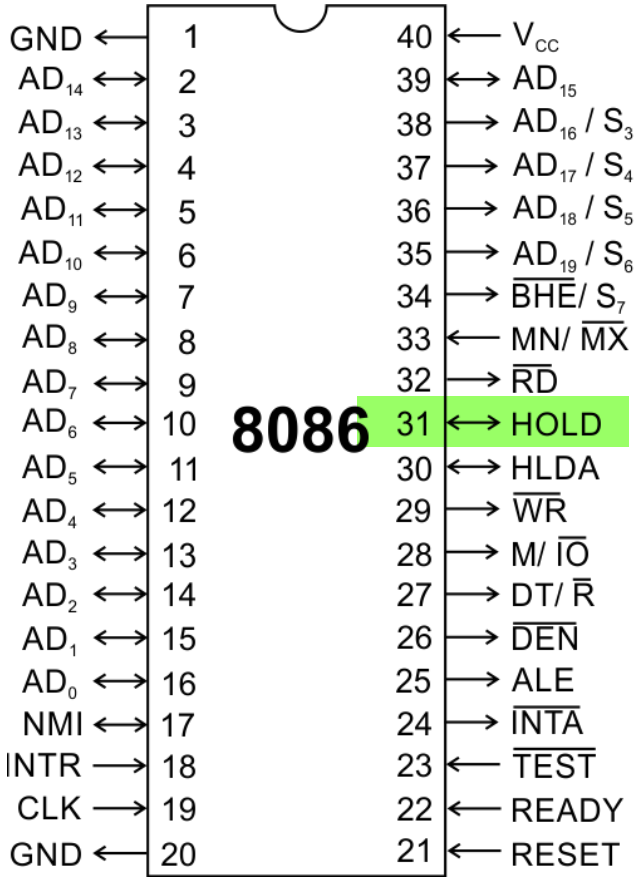
M/$\overline{IO}$ — Used to differentiate memory access and I/O access. For memory reference instructions, it is high. For IN and OUT instructions, it is low.

$\overline{WR}$ — Write control signal; asserted low Whenever processor writes data to memory or I/O port

$\overline{INTA}$ — (Interrupt Acknowledge) When the interrupt request is accepted by the processor, the output is low on this line.

Pins and Signals

Minimum mode signals



Pins 24 -31

For minimum mode operation, the MN/ $\overline{MX}$ is tied to VCC (logic high)

8086 itself generates all the bus control signals

HOLD — **Input signal to the processor form the bus masters as a request to grant the control of the bus.**

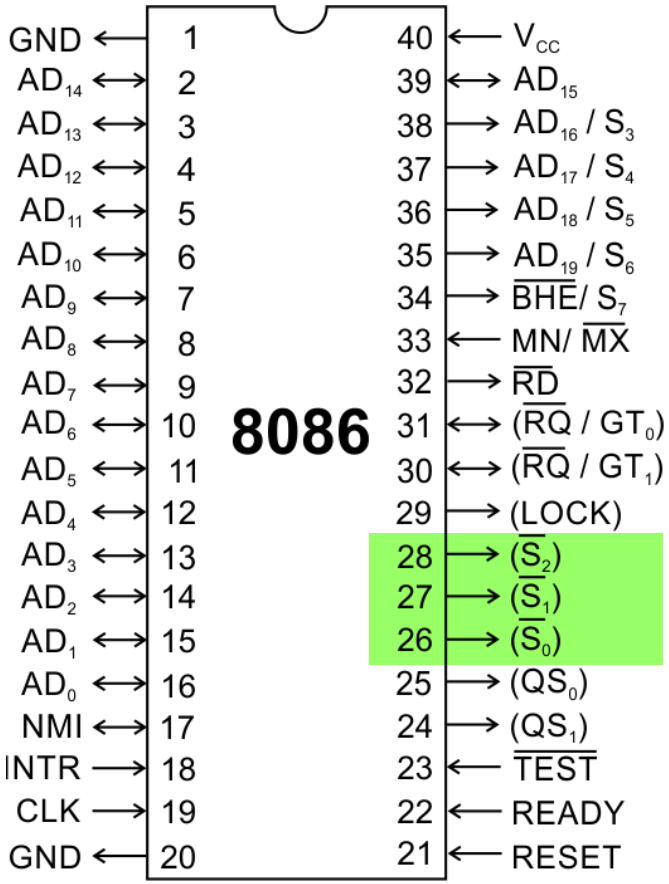
Usually used by the DMA controller to get the control of the bus.

HLDA — **(Hold Acknowledge) Acknowledge signal by the processor to the bus master requesting the control of the bus through HOLD.**

The acknowledge is asserted high, when the processor accepts HOLD.

Pins and Signals

Maximum mode signals



During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned

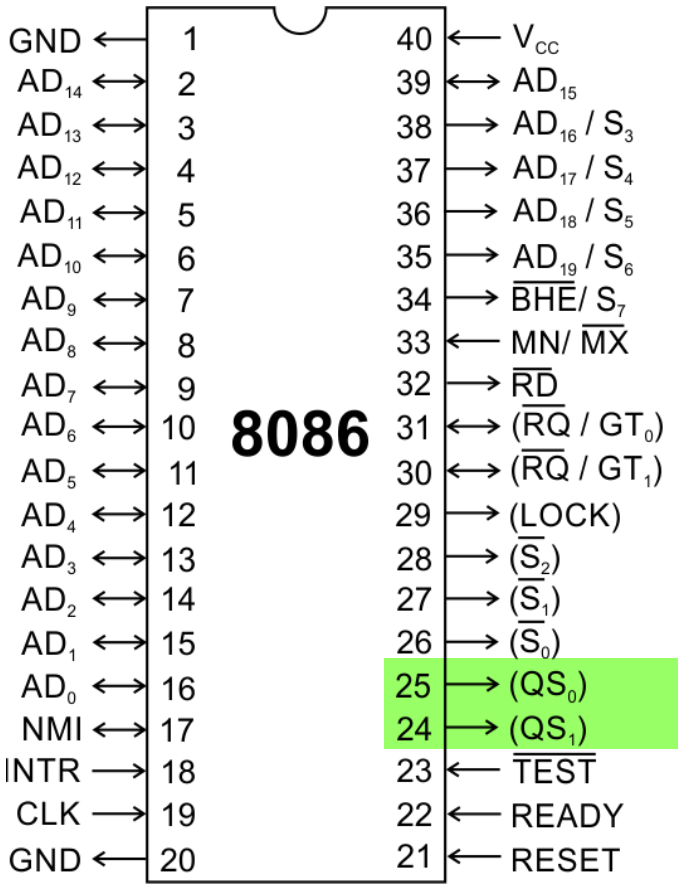
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Status signals; used by the 8086-bus controller to generate bus timing and control signals. These are decoded as shown.

Status Signal			Machine Cycle
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive/Inactive

Pins and Signals

Maximum mode signals



During maximum mode operation, the MN/ $\overline{MX}$ is grounded (logic low)

Pins 24 -31 are reassigned

$\overline{QS_0}$, $\overline{QS_1}$

(Queue Status) The processor provides the status of queue in these lines.

The queue status can be used by external device to track the internal status of the queue in 8086.

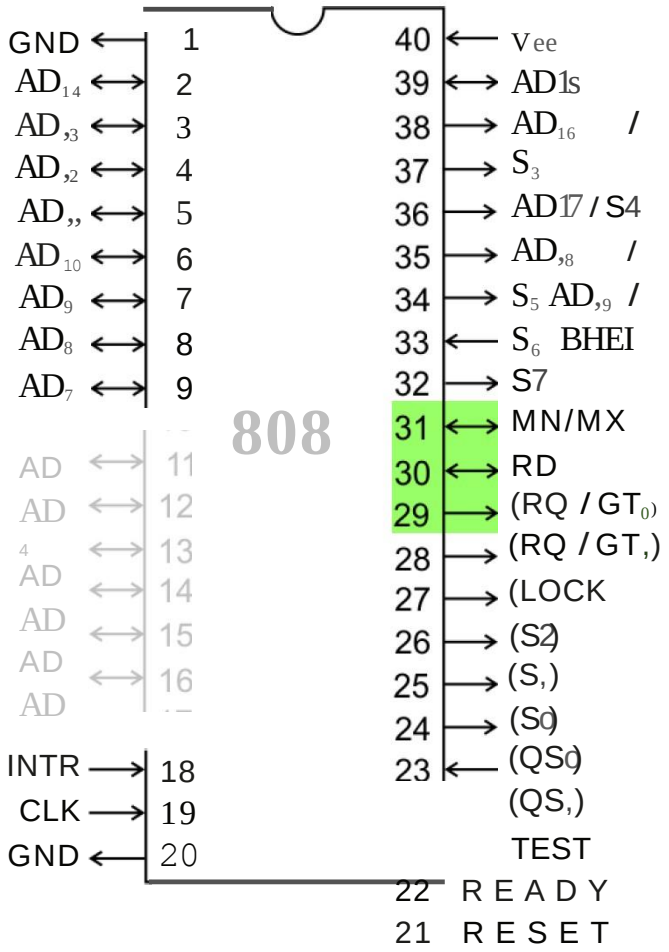
The output on QS_0 and QS_1 can be interpreted as shown in the table.

Queue status		Queue operation
QS_1	QS_0	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Pins and Signals — Maximum mode signals

During maximum mode operation, the MN/ MX is grounded (logic low)

Pins 24 -31 are reassigned



HQt GT0
'RQ/ (J1

(Bus Request/ Bus Grant) These requests are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle.

These pins are bidirectional.

The request on f/10 will have higher priority than
(/fl

LOCK

An output signal activated by the LOCK prefix instruction.

Remains active until the completion of the instruction prefixed by lOCK.

The 8086 output low on the LOCK pin while executing an instruction prefixed by LOCK to prevent other bus masters from gaining control of the system bus.

Thank you so much

Any questions ?