Ministry of Higher Education and
Scientific Research - Iraq
University of Diyala
College of Engineering
Department of Computer Engineering

الملحق ٤: وصف المادة الدراسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Logic Circuits Design**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☒ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**CPE 106**				
ECTS Credits	**5**				
SWL (hr/sem)	**125**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Computer Eng.		**College**	College of Engineering	
Module Leader	Dr. HUSSAIN FALIH MAHDI		**e-mail**	dr.hussain.mahdi@uodiyala.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Ahmed Salah Hameed		**e-mail**	ahmedhameed_eng@uodiyala.edu.iq	
Scientific Committee Approval Date	26/12/2023		**Version Number**	1.1	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	Principles of Logic Systems	**Semester**	1
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. To acquire the basic knowledge of combinational and sequential logic circuits. 2. Have a thorough understanding of different logic circuits and its applications. 3. To help students understand the design of complex digital circuits. 4. Ability to identify basic requirements for a design application and propose a cost-effective solution. 5. To prepare students to perform the analysis and design of various digital electronic circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Students will be able to describe the strengths and weaknesses of different logic circuits and select the appropriate design for a given problem. 2. Students will be able to communicate effectively about their designs, both orally and in writing. 3. Students will be able to work effectively in teams to design and implement combinational and sequential digital circuits. 4. Students will be able to apply the principles of sequential logic design to more complex problems. 5. Students will be able to assess the performance and reliability of digital systems. 6. Students will be able to learn independently and continue to develop their knowledge and skills in the field of logic design.
Indicative Contents المحتويات الإرشادية	- Overview to Combinational Logic circuits [3 hrs] - Combinational Logic circuits design. [27 hrs] - Introduction to sequential logic circuits [3 hrs] - Flip-Flops and it's applications [9 hrs] - Counters [3 hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, homework's and examples. Practical examples helps students to understand the course material.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	**79**	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	**5**
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	**46**	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	**3.1**
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	**2**	**10% (10)**	**6 and 13**	**LO #1 to #3 and #4 to #6**
	Assignments	**2**	**10% (10)**	**4 and 12**	**LO #2 and #3 to #5**
	Projects / Lab.	**1**	**10% (10)**	**Continuous**	**All**
	Report	**1**	**10% (10)**	**13**	**LO #4 to #6**
Summative assessment	**Midterm Exam**	**2hr**	**10% (10)**	**8**	**LO #1 - #5**
	Final Exam	**3hr**	**50% (50)**	**16**	**All**
Total assessment			**100% (100 Marks)**		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Overview to Combinational Logic circuits
Week 2	Adders and Subtractors circuits
Week 3	Series and Parallel Binary Adders circuits
Week 4	Ripple carry versus Parallel Look-Ahead Carry Adders circuits
Week 5	Binary multiplier circuits and Magnitude comparators circuit.
Week 6&7	Encoders, and Decoders circuits
Week 8&9	Multiplexers, and Demultiplexers circuits.
Week 10	Parity Generators/Checkers and design of code conversion circuits.
Week 11	Introduction to sequential logic circuits
Week 12-14	Flip-Flops:(Latches, Edge-Triggered Flip-Flops) and it's applications.
Week 15	Counters
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction to logic gates
Week 2	Lab 2: NOR Gate, NAND Gate, and XOR Gate application
Week 3	Lab 3: Comparator Circuit
Week 4	Lab 4: Half –Adder
Week 5	Lab 5: full –Adder Circuit
Week 6	Lab 6: Half Subtractor
Week 7	Lab 7: full Subtractor Circuit
Week 8	Lab 8: Even and odd Parity Generator and Checker Circuit
Week 9	Lab 9: Code converter Circuits
Week 10	Lab 10: Encoder Circuit
Week 11	Lab 11: Decoder Circuit
Week 12	Lab 12: Multiplexer Circuit

Week 13	Lab 13: De - Multiplexer Circuit.
Week 14	Lab 14: Flip- Flop application Circuits
Week 15	Lab 15: Counters

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Robert L. Boylestad and Louis Nashelsky, Electronic Devices and Circuit Theory, 7th or 10th or 11th Edition.	Yes
Recommended Texts	• Charles K. Alexander and Matthew N. O. Sadiku, Fundamentals of Electric Circuits, McGrawHill, fourth edition, 2009.Behzad Razavi, *Fundamentals of Microelectronics*, John Wiley & Sons, Preview Edition, 2006 • J J Kathy and SA Naser, fundamental of Electrical Engineering, Schaum's outline, Academia International, 2004. • Any other materials available on the web.	No
Websites	https://www.youtube.com/playlist?list=PLHCD1a8slQtKqkfG5FISKwHxVzkptxZVR	

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.