الملحق ٤: وصف المادة الدراسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information
معلومات المادة الدراسية

Module Title	**Digital Electronics**	**Module Delivery**	
Module Type	Core	☒Theory	
Module Code	**CPE 204**	☒Lecture	
ECTS Credits	6	☒ Lab	
SWL (hr/sem)	150	☐Tutorial ☐Practical ☐Seminar	

Module Level	2	**Semester of Delivery**	3
Administering Department	Computer Eng.	**College**	College of Engineering
Module Leader	Royida A. Ibrahem	**e-mail**	royida.alhayali@uodiyala.edu.iq
Module Leader's Acad. Title	Lecturer	**Module Leader's Qualification**	MCS
Module Tutor	Name (if available)	**e-mail**	E-mail
Peer Reviewer Name		**e-mail**	
Scientific Committee Approval Date	02/06/2024	**Version Number**	1.0

Relation with other Modules
العلاقة مع المواد الدراسية الأخرى

Prerequisite module	CPE 106	**Semester**	2
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents	
أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	Upon completion of this course, the student will be able to: 1. - Learn how to deal with flip flops. 2. Learn how to develop meter design. 3. Familiarity with the basic concepts of the types and types of transfer records. 4. Familiarity with the method of designing information transfer circuits as well as logical programmed devices. 5. The student learns the types of programmed logic devices as well as sequential logic circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Enabling the student to understand the basic concepts and structure of counters, including their types and applications. 2. Enabling the student to learns the conversion registers. 3. Enabling the student to understand the solutions of problems related to Learn programmable logic devices, programmable logic arrays. 4. Enabling the student to learn about diodes and their types.
Indicative Contents المحتويات الإرشادية	1. Introduction to the types of synchronous and asynchronous counters, the cascade counter and counter applications. (6 Hrs) 2. The conversion register, its types and applications. (6 Hrs) 3. Information conversion circuits, their types and applications. the diodes and their types. (12 Hrs) 4. Programmable logic devices, programmable logic arrays, general matrix logic, and an introduction to sequential logic circuits. (21 Hrs)

Learning and Teaching Strategies	
استراتيجيات التعلم والتعليم	
Strategies	• The lecturer prepares lectures on the subject in paper and electronic form and presents them to the students. • The lecturer delivers lectures in detail. • The lecturer requests periodic reports and homework assignments on the basic topics of the subject.

Student Workload (SWL)

الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	78	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعيا	5.2
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	72	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعيا	4.8
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	20% (10)	6 and 14	LO #1 to #4
	Assignments	2	10% (5)	4, 7 and 10	LO #1, #2 and #5
	Projects / Lab.	1	10% (10)		
	Report				
Summative assessment	Midterm Exam	1 hr	10% (10)	9	LO #1 to #3
	Final Exam	3 hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Overview about introduction to the types of synchronous counters.
Week 2	Overview about introduction to the types of asynchronous counters.
Week 3	The cascade counter.
Week 4	Counter applications.

Week 5	Conversion register, its types and applications(Kinds of Shift register).
Week 6	Shift register Applications.
Week 7	Data Conversion circuits: Analog to Digital Conversion (ADC) ,ADC methods.
Week 8	ADC methods.
Week 9	Digital to Analog Conversion (DAC), DAC methods.
Week 10	DAC methods.
Week 11	Diode–Transistor–Logic.
Week 12	Programmable Logic Devices.
Week 13	Programmable Logic Array (PLA).
Week 14	Programmable Array Logic.
Week 15	Introduction Sequential Logic Circuit.
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Introduction to using the software.
Week 2	Synchronous counters.
Week 3	Synchronous counters.
Week 4	Asynchronous counters.
Week 5	Asynchronous counters.
Week 6	Kinds of Shift register
Week 7	ADC methods.
Week 8	ADC methods.
Week 9	DAC methods.
Week 10	DAC methods.
Week 11	Diode–Transistor–Logic.
Week 12	Programmable Logic Devices.
Week 13	Programmable Logic Array (PLA).
Week 14	Programmable Array Logic.
Week 15	**Preparatory week before the final Exam**

Learning and Teaching Resources

مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Thomas l. Floyd, DIGITAL FUNDAMENTALS,	Yes
Recommended Texts	• Anil K. Maini, Digital Electronics Principles, Devices and Applications. • M. Morris Mano, Digital Design, • Sir.C.V.Raman Nagar, Tirunelveli-12, Digital Principles and System Design. • John Crowe and Barrie Hayes-Gill, Introduction to Digital Electronics.	No
Websites		

Grading Scheme

مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.