Ministry of Higher Education and Scientific Research - Iraq
University of Diyala
College of Engineering
Department of Computer Engineering

الملحق ٤: وصف المادة الدراسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Computer Architecture**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☒**Lecture** ☐**Lab** ☐**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	**CPE 207**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	2		**Semester of Delivery**	4	
Administering Department	Computer Eng.		**College**	College of Engineering	
Module Leader	Ahmed Salah Hameed		**e-mail**	ahmedhameed_eng@uodiyala.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	PhD	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date	02/06/2024		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	CPE 106	**Semester**	2
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	Upon completion of this course, the student will be able to: 1. Understanding the basic concepts and structure of computers. 2. Exploring register transfer logic, arithmetic operations, and addressing modes. 3. Learning about memory organization, memory hierarchy design, and instruction execution stages. 4. Understanding micro operations, hardwired control, micro programmed control, and computer arithmetic operations. 5. Learning about parallel processing, pipelining, and Multi-processor concepts.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Enabling the student to understand the basic concepts and structure of computers, including computer organization, processor principles. 2. Enabling the student to analyze the behavior of the main components of a computer system. 3. Enabling the student to manage the computer memory and memory hierarchy. 4. Enabling the student to understand the solutions of problems related to modern processor cores, including instruction routing, pipelining, and performance optimization. 5. Enabling the student to learn about parallel processing, multi-processor systems, and GPUs.
Indicative Contents المحتويات الإرشادية	• Overview about digital computer system architecture(3 hrs), • Register transfer language; Bus and memory transfers(3 hrs), • Arithmetic micro-operations and Logic micro-operations(3 hrs), • Basic computer organization and design(3 hrs), • Micro-programmed control memory; Control memory(3 hrs), • Central processing unit. General register organization(3 hrs), • Fundamentals of parallel processing(3 hrs), • Pipelining: Basic and Intermediate Concepts(3 hrs), • Instruction pipeline. RISC Pipeline(3 hrs), • Memory Hierarchy Design(3 hrs), • Cache performance optimization(3 hrs), • Virtual memory(3 hrs), • Multiprocessors and Thread-Level Parallelism(3 hrs), • Cache Coherence in Multiprocessor systems(3 hrs), • Basic of SIMD Processors and GPUs(3 hrs),

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, homework's and examples. Practical examples helps students to understand the course material.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	**48**	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	**3.2**
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	**102**	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	**6.8**
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	**2**	**20% (10)**	**6 and 14**	**LO #1 to #4**
	Assignments	**2**	**10% (5)**	**4, 7 and 10**	**LO #1, #2 and #5**
	Class Work	**2**	**10% (5)**		
	Report				
Summative assessment	**Midterm Exam**	**1 hr**	**10% (10)**	**9**	**LO #1 to #3**
	Final Exam	**3 hr**	**50% (50)**	**16**	**All**
Total assessment			**100% (100 Marks)**		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Overview about digital computer system architecture.
Week 2	Register transfer language; Bus and memory transfers.
Week 3	Arithmetic micro-operations and Logic micro-operations.
Week 4	Basic computer organization and design.
Week 5	Micro-programmed control memory; Control memory.
Week 6	Central processing unit. General register organization.
Week 7	Fundamentals of parallel processing
Week 8	Pipelining: Basic and Intermediate Concepts
Week 9	Instruction pipeline. RISC Pipeline
Week 10	Memory Hierarchy Design
Week 11	Cache performance optimization
Week 12	Virtual memory
Week 13	Multiprocessors and Thread-Level Parallelism
Week 14	Cache Coherence in Multiprocessor systems
Week 15	Basic of SIMD Processors and GPUs
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	
Week 2	
Week 3	
Week 4	
Week 5	
Week 6	
Week 7	

Week 8	
Week 9	
Week 10	
Week 11	
Week 12	
Week 13	
Week 14	
Week 15	

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	• Morries Mano, Computer System Architecture, 3rd edition, 1993 • John L. Hennessy and David A. Patterson, Morgan Kaufmann, Computer Architecture: A Quantitative Approach, 5th Edition, 2011, ISBN: 9780123838728.	Yes
Recommended Texts	• J.L. Hennessy and D.A. Patterson. Computer Architecture: A Quantitative Approach, 5th Edition, Morgan Kaufmann, 2012. • J.P. Shen and M.H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors. McGraw-Hill Higher Education, 2004. (Chapter 5 in course packet) • Bryant, Randal E. and O'Hallaron, David R., Computer Systems: A Programmer's Perspective, 2nd Edition Prentice Hall, 2011. • A.B. Downey. Think Python: How to Think Like a Computer Scientist, version 2.0.13. O'Reilly, 2014. • C. Fletcher, EECS150: Interfaces FIFO (a.k.a Ready/Valid). UC Berkeley, 2009.	No
Websites		

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.